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3D LORAN-C NAVIGATOR DOCUMENTATION.(U)

JAN 82 E H BOLZ, L D KING

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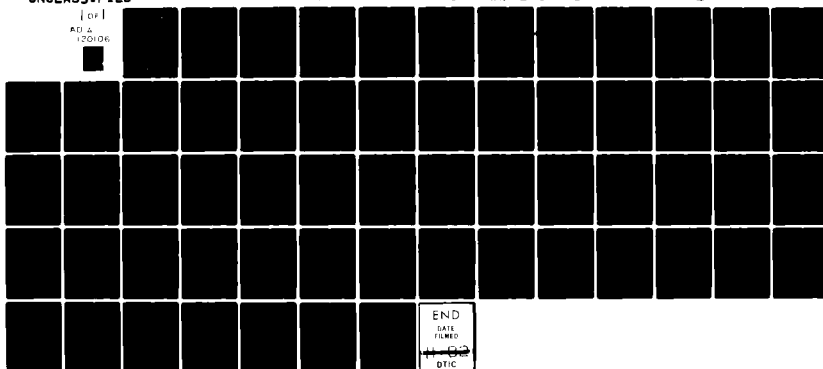
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3D Loran-C Navigator Documentation

Eric H. Bolz
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Final Report

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Technical Report Documentation Page

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<p>16. Abstract</p> <p>The purpose of this task was to develop a 3D Loran-C Navigator by configuring an interface unit between an airborne Loran-C navigator (Teledyne TDL-711) and an Altitude Alerter/VNAV Guidance system (Intercontinental Dynamics model 541). The digital computer-based interface unit was designed to allow the flight crew to specify the approach slope (3.0 to 9.9 degrees). This report documents the hardware and software in the interface unit, and interconnection with the other involved systems.</p> <p>The availability of accurate, three-dimensional approach guidance information at airports where no ILS is available provides significant operational advantages, to helicopter operators in particular. The 3D Loran-C navigator system was bench tested and flight demonstrated. Smooth, accurate (within the limitations of Loran-C) descent guidance information was obtained.</p>			
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METRIC CONVERSION FACTORS

Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
LENGTH				
m	inches	2.5	centimeters	cm
ft	feet	30	centimeters	cm
y	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
AREA				
sq in	square inches	6.5	square centimeters	cm ²
sq ft	square feet	0.09	square meters	m ²
sq yd	square yards	0.8	square meters	m ²
sq mi	square miles	2.6	square kilometers	km ²
ac	acres	0.4	hectares	ha
MASS (weight)				
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons	0.9	tonnes	t
	(2000 lb)			
VOLUME				
cup	teaspoons	5	milliliters	ml
fl oz	tablespoons	15	milliliters	ml
qt	fluid ounces	30	milliliters	ml
pt	cups	0.24	liters	l
qt	quarts	0.47	liters	l
gal	gallons	0.95	liters	l
cu ft	cubic feet	3.3	liters	l
cu yd	cubic yards	0.03	cubic meters	m ³
		0.76	cubic meters	m ³
TEMPERATURE (exact)				
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

* 1 m = 2.54 (exact). For other exact conversions and more detailed tables, see NBS Mon. Publ. 286, Units of Lengths and Measures, Price \$7.25, SD Catalog No. C1310-286.

Symbol	When You Know	Multiply by	To Find	Symbol
LENGTH				
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
y	yards	1.1	yards	yd
km	kilometers	0.6	miles	mi
AREA				
cm ²	square centimeters	0.16	square inches	in ²
m ²	square meters	1.2	square yards	yd ²
ha	square kilometers	0.4	square miles	mi ²
km ²	hectares (10,000 m ²)	2.5	acres	ac
MASS (weight)				
g	grams	0.005	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	st
VOLUME				
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
m ³	liters	0.26	gallons	gal
m ³	cubic meters	35	cubic feet	cu ft
m ³	cubic meters	1.3	cubic yards	cu yd
TEMPERATURE (exact)				
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F

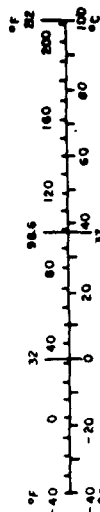


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1.0 3D LORAN-C NAVIGATOR FUNCTIONS AND SOFTWARE

1.1 INTRODUCTION

The concept which motivated the development of this device was to be able to conduct instrument approach procedures with let-down guidance at airports or landing sites which have no ILS glideslope equipment. This capability requires the availability of an area coverage navigation sensor with good accuracy and stability, such as Loran-C, and other instrumentation required to process altitude and position data in order to calculate command descent guidance. At present there is no commercially available Loran-C navigator which provides 3D (VNAV) guidance. In order to demonstrate the 3D Loran-C capability, hardware was developed to interface a popular Loran-C navigator (the Teledyne TDL-711) to a commercially-available approach guidance computer and altimeter (the model 541 VNAV/ALERTER made by Intercontinental Dynamics). This hardware is discussed in detail in Section 2.

1.2 SYSTEM INTERFACE REQUIREMENTS

The major problem addressed by this system was to resolve the interface incompatibility between the TDL-711 navigator and IDC VNAV system. The normal input provided to the IDC VNAV in an ordinary installation, where it is connected to a DME or an RNAV computer, is a D.C. voltage analog of distance to station/or waypoint. The TDL-711 is designed to drive a standard localizer needle, localizer flag and TO/FROM flag, and has no outputs for other aircraft instrumentation, in particular, no output intended to drive a distance to waypoint (DTW) display. The TDL-711 does have two digital data ports. The first is dedicated to communications with the associated control/display unit (CDU). The second is intended for driving a remote display unit (RDU), which repeats the data displayed on the CDU. The data content of the RDU data stream is, however, modifiable through parameters stored on an EPROM. This fact has been used to advantage in flight test programs conducted by SCT, FAATC and DOT/TSC. A version of the EPROM was developed several years ago for NASA LRC which has been used in most of these tests. It causes the RDU data port to generate a long (157 bytes) stream of data which is then recorded by the

airborne data acquisition system. One of the elements in that data stream is distance to waypoint (DTW) in BCD format in units of nautical miles and tenths. The task of the interface unit provided under this contract was to accept the RDU data format which is periodically transmitted, extract the DTW data (and other related information), and generate a smooth, accurate D.C. analog representation of aircraft distance to waypoint to drive the VNAV computer. A further function was to provide approach guidance at a selectable glideslope angle (up to 9.9°), rather than just the fixed 3° built into the VNAV.

1.3 LORAN-C OUTPUT DATA CHARACTERISTICS

Since the TDL-711 was not conceived with the intention of driving a remote DTW indicator (let alone a VNAV descent guidance computer), the output data which is available requires extensive processing to result in suitable guidance data. The form of the output data is binary coded decimal in units of one-tenth nautical mile. This resolution is not sufficiently fine to directly control descent guidance. At a 6° approach angle, a 0.1 nm resolution yields a 64 foot vertical guidance resolution. The scale factor of the IDC VNAV is 20 ft per dot deflection, so the discontinuity would be in excess of 3 dots. The nominal data update rate of the TDL-711 is roughly once per second. However, it has been found in earlier flight evaluations that this rate can be variable, and interruptions to the data stream of several seconds can result. Additional parameters in the output data stream can be used to determine when waypoints have been sequenced, or if the navigator is unable to track the Loran-C signal. These factors should control the presence of the glideslope flag.

It was apparent from the outset that some form of digital filtering scheme should be applied within the interface unit in order to track and smooth the data. The use of True Airspeed data as an aid to the filtering process was considered. However, Loran-C receivers typically have no provision for airspeed input (it is not necessary for tracking the time difference signals, even at high velocities). Furthermore, many of the types of aircraft which would find a Loran-C 3D approach system useful (in particular helicopters) do not have an electrical

airspeed signal on board. Therefore, the only data available is the Loran-C DTW information itself. In order to avoid tracker standoff errors, a second order alpha-beta tracker algorithm was implemented. This set of equations estimates velocity as well as position, and requires an initial guess of velocity to start tracking. This is provided through a set of jumper wires which may be changed as required for a given aircraft performance.

1.4 TRACKER ALGORITHM

The alpha-beta (α - β) tracker technique is tailored to tasks involving real-time tracking of data where knowledge of probable future behavior is limited, and where no redundant data sources are available. Its design is based on assumptions regarding (1) the accuracy of the data representing the physical entity being tracked (in this case the Loran-C DTW is the data and the physical entity is flight progress along the path), and (2) probable future behavior of the entity being tracked. The representation of accuracy is the standard deviation of the measurement error. The representation of probable future behavior is the standard deviation of the longitudinal acceleration expected of the aircraft as it conducts an instrument approach.

The philosophy behind the α - β tracker is discussed in further detail in Reference 5. The equations for computing the optimal gains (α and β values) are presented there. The gains are functions of three values, the standard deviation of measurement error, the standard deviation of acceleration, and the time between updates. Based on earlier flight test experience with Loran-C, it was assumed that the Loran-C random error component (repeatability) would be 300 ft (0.05 nm). In addition, the granularity of the data (0.1 nm) introduces an error whose S.D. = 0.03 nm. These values were RSS added to yield an overall measurement error estimate of 0.06 nm. Based on earlier experimental tracker development work^[5], it was assumed that the standard deviation of longitudinal acceleration was 0.1 g. As previously mentioned, the time between updates is a variable. The

α and β gain equations were solved for several values of update interval, with results shown in Table 1.1.

Table 1.1 α and β Gains Versus Update Interval

Δt	1	3	5	10
α	.121	.321	.474	.719
β	.0078	.0206	.0302	.0442

Linear approximations of gain values versus update interval have been estimated, as follows:

$$\alpha = 0.05447 + 0.0664\Delta t$$

$$\beta = 0.0039 + 0.0039\Delta t$$

As implemented in the interface unit, the update interval is calculated as the difference in arrival times of two successive Loran-C data streams. Each time a Loran-C data block is received, the gains are calculated based on the update rate. The gains are used to estimate new distance and velocity values using the following equations:

$$\left. \begin{aligned} \hat{\dot{x}}(n+1) &= \hat{\dot{x}}(n) + \Delta t \hat{\ddot{x}}(n) \\ \hat{\ddot{x}}(n+1) &= \hat{\ddot{x}}(n) \end{aligned} \right\} \text{Prediction Equations}$$

$$\left. \begin{aligned} \hat{x}(n) &= \hat{\dot{x}}(n) + \alpha(D(n) - \hat{\dot{x}}(n)) \\ \hat{\ddot{x}}(n) &= \hat{\ddot{x}}(n) + \beta(D(n) - \hat{\dot{x}}(n)) \end{aligned} \right\} \text{Smoothing Equations}$$

Given, at any update n , a value for distance estimate $\hat{x}(n)$ and velocity estimate ($\hat{\dot{x}}(n)$), the predicted distance $\hat{\dot{x}}(n+1)$ and velocity $\hat{\ddot{x}}(n+1)$ at the next update $n+1$ are given by the prediction equations. Once predicted values ($\hat{\dot{x}}, \hat{\ddot{x}}$) are known for an update n , the measured distance $D(n)$ is used to smooth and update the tracker yielding estimated

distance $\hat{x}(n)$ and velocity $\hat{\dot{x}}(n)$, using the smoothing equations and the calculated values for α and β . To start the process:

$$\hat{x}(1) = D(1)$$

$$\hat{\dot{x}}(1) = \text{Value programmed using jumpers}$$

This is done at any point that the software chooses to reset (discussed in the next section). In between updates, the distance to waypoint value sent to the D/A output device is calculated using the prediction equations. The value for Δt used is time since the last update. This value is updated sixteen times per second. A second D/A channel is used to generate the DME valid flag signal (+16 VDC is valid, 0 is invalid).

1.5 OPERATIONAL SOFTWARE

The software for the 3D Loran-C Navigator interface unit is written in Intel 8080 Assembly Language. The object code has been programmed into a 2716 EPROM located at board position U102. The Monolithic Systems Uniform Monitor EPROM is located at position U101. Upon power-up or system reset, the program in the Uniform Monitor executes, which transfers control to the interface program in U102. The first function of this program is to move the entire program into RAM (random access memory) at location 8040H (hexidecimal) where it executes. The Assembly Listing in Figure 1.1 shows the code as assembled to load at location 8040. Once loaded, no further use of the EPROM at U102 is made. Several subroutines in the monitor at U101 are used in many places in the interface program.

The interface unit program consists of the following sections:

- 1) Data Area Initialization 8040H
 - Initializes all data areas, addresses and pointers used by the program (this section is not executed).
- 2) Monitor Set-Ups 80A4H
 - Completes initializations normally performed by the Monitor (copied from the MSC Uniform Monitor listing)

PROGRAM LORANTV -- DERIVATIVE SMOOTHED DFM FROM TDL-71 RDU DATA
11/2/01/88)

Figure 1.1 3D Lorān-C Navigator Assembly Listing

8099 0000	B16	DM 0000H	! ALPHA GAIN OFFSET	! ALPHA-BETA
8098 0E00	ALPHA0	DM 000FH	! ALPHA GAIN TIME SENSITIVITY	! TRACKER GAINS
809D 1100	ALPHA1	DM 0111H	! BETA GAIN OFFSET X256	
809F 0001	BETA0	DM 0100H	! BETA GAIN TIME SENSITIVITY X256	
80A1 0001	BETA1	DM 0100H	! SIGN SAVER FOR MULTIPLY (M1616)	
80A3 00	SIGN	DB 03H		
80A4 21B400	START	LXI H, 00B4H	! MONI: PRESET "GO" ADDR	! COMPUTER HARDWARE AND SOFTWARE
80A7 2227FF		SHLD OFF27H	! STD:	! INITIALIZATIONS, COPIED FROM
80AA C01481		CALL BAUDA	! INITIALIZE MAIN PORT	! MSC UNIVERSAL MONITOR PROGRAM
80AD C03106		CALL 0631H	! CNT: INIT I/O	
80B0 2100FF		LXI H, OFF00H	! RMORG:	
80B3 2231FF		SHLD OFF31H	! RSP: PRESET USER STACK	
80B6 C00607		CALL 0706H	! MSG1:	
80B9 00DA4C4F52		DB 0DH, 0AH, 07, 00H		
80C3 21E0FF			! INIT RST VECs TO POINT AT BKPT	
80C6 114701		LXI H, OFFE0H	! VECs:	
80C9 0EC3		LXI D, 0147H	! BKPT:	
80CB 0608		MVI C, 0C3H	! JMP1:	
80CD 71	MORP	MVI B, 08H		
80CE 23		MOV M, C	! STORE JUMP OP CODE	
80CF 73		INX H		
80D0 23		MOV M, E	! STORE BKPT PTR	
80D1 72		INX H		
80D2 23		MOV M, D		
80D3 05		INX H		
80D4 C2C080		DCR B	! DJNZ:	
80D7 31E0FF		JNZ MONP	! LOOP TILL VECs ALL FIXED	
80DA AF				
80DB 3200FF		LXI SP, OFFE0H	! MONSR: PRESET STACK	
80DE C05281		XRA A	! EF:	
80E1 C03981		STA OFF00H		
80E4 C05581			! MONITOR SETUPS COMPLETE	
80E7 C09281		CALL BAUDB	! SET PORT B BAUD RATE	
80EA C0F080		CALL PARSET	! SETUP PARALLEL PORTS & READ SPEED	
80ED C36482		CALL PSETUP	! PATCH INTERRUPT ADDRESSES	
80F0 3E01	CSETUP	CALL CRESET	! RESET CLOCK	
80F2 327180		CALL CSETUP	! SETUP CLOCK INTERRUPT, START CLOCK	
80F5 AF		JMP MAIN	! START DTM TRACKING	
80F6 327280				

! JUMP TO MAIN ROUTINE
 ! INITIALIZATION ROUTINES FOLLOW
 ! SET UP SYSTEM REAL TIME CLOCK
 ! USES INTERRUPT 7. INTERRUPT IS
 ! GENERATED EVERY 1/256TH SECOND

! END OF SECTION COPIED FROM MONITOR
 ! SOFTWARE INITIALIZATIONS

Figure 1.1 - Continued

80F9 32/380	STA 0000H	INTERRUPT / VECTOR ADDR
80FC 21F3FF	LXI H, 0FF3H	IN NEW INTERRUPT 7 JUMP ADDR
80FF 119C81	LXI D, 17ADR	
8102 73	MOV M, E	
8103 23	INX H	
8104 72	MOV M, D	JMP TO 17ADR FOR INTERRUPT
8105 3E70	MVI A, 70H	1 01 11 000 0 TIMER BYTE
8107 D3FF	OUT 0DFH	1CTR1 28YT MIDEO BNR
8109 2A6080	LHLD INTRVL	1TIMER CHIP CONTROL PORT
810C 7D	MOV A, L	1 = 1/256 OF SECOND
810D D3DD	OUT 0DDH	1TIMER 1 PORT
810F 7C	MOV A, H	
8110 D3DD	OUT 0DDH	
8112 3E08	MVI A, 08H	1SET Z80 MODE 0. NO PRIORITY.
8114 D377	OUT 0D7H	1INTERRUPT CONTROLLER REGISTER
8116 FB	EI	1START CLOCK
8117 C9	RET	
8118 3E96	BAUDA	1 10 01 001 0
811A D3FF	OUT 0DFH	1CTR2 LSB MODE3 BNR
811C 3E68	MVI A, 068H	1SET COUNTER 2 MODE
811E D3DE	OUT 0DEH	11200 BAUD
8120 3E80	MVI A, 80H	1COUNTER 2 REGISTER
8122 D3DD	OUT 0EDH	1RESET PORT
8124 3E80	MVI A, 80H	1PORT A CONTROL/STATUS BYTE
8126 D3DD	OUT 0EDH	
8128 3E40	MVI A, 40H	
812A D3DD	OUT 0EDH	
812C 3ECE	MVI A, 0CEH	
812E D3DD	OUT 0EDH	
8130 3E37	MVI A, 37H	
8132 D3DD	OUT 0EDH	
8134 D3ED	IN 0EDH	
8135 D3FC	IN 0EDH	
8138 C9	RET	
8139 3E9B	PARSET	1SET ALL PARALLEL PORTS TO INPUT
813B D3E7	OUT 0E7H	18255 CONTROL PORT
813D D3E5	IN 0E5H	1PARALLEL PORT B (INITIAL
813F 2F	CMA	1A/C SPEED ESTIMATE)
8140 E0FF	ANI 0FH	1COMPLEMENT
8142 328180	STA PHOGSP	1LOW ORDER FOUR BITS
		1SAVE IT
		1INITIALIZE PARALLEL PORTS FOR INPUT

Figure 1.1 - Continued

8145 210000	LXI H, 0000H	12F0 DISTANCE	1 INITIALIZE ANALOG BOARD
8146 220477	SHLD 07704H	1 FLAG IN VIEW VALUE	
8148 213303	LXI H, 0313H	1 RESET ANALOG BOARD	
814E 220677	SHLD 07706H		
8151 C9	RET		
8152 3E16	BAUD8	1 SET PORT B BAUD RATE	1 PORT B RECEIVES TDL-711 DATA STREAM
8154 D31F	OUT 0DFH	1 00 01 011 0	
8156 0E06	MVI C, 006H	1 CTRO LSH MODE3 BNR	
8158 DB5	IN 0E5H	1 SET COUNTER 0 MODE	1 TDL-711 BAUD RATE
815A E610	ANI 10H	1 = 20933 BAUD	1 BIT 4 NOT SET SIGNALS
815C C26181	JNZ BAUD81	1 PARALLEL PORT B (BAUD SELECT)	1 TEST SET-UP (4800 BAUD)
815F 0E1A	MVI C, 01AH	1 BIT 4	
8161 79	MOV A, C	1 = 4800 BAUD	
8162 030C	OUT 0DCH	1 COUNTER 0 REGISTER	
8164 C9	RET		
8165 21F0FF	PSETUP	1 INTERRUPT 6 VECTOR ADDRESS	1 SET UP INTERRUPT SCHEME TO
8168 11D381	LXI H, 0FF0H		1 RECEIVE LORAN-C DATA STREAM
816B 73	LXI D, 16A0H		
816C 23	MOV M, E		
816D 72	INX H	1 PATCH ADDR IN TABLE	
816E AF	MOV M, D		
816F 32/280	XRA A	1 INITIALIZATIONS	
8172 32/380	STA 0010H		
8175 3C	STA 000E		
8176 32/180	INR A		
8179 3E60	STA 5050H	1 RESET PORT B	1 BAUD RATE SET UP BY BAUD8 ROUTINE
817B D3CF	MVI A, 80H		
817D 3E82	OUT 0CFH		
817F D3CF	MVI A, 80H		
8181 3E40	OUT 0CFH		
8183 D3CF	MVI A, 40H		
8185 3ECE	OUT 0CFH		
8187 D3CF	MVI A, 0CEH		
8189 3E37	OUT 0CFH		
818B D3CF	MVI A, 037H		
818D D3CF	OUT 0CFH		
818F D3CF	IN 0CFH		
8191 C9	IN 0CFH		
8192 216280	CHREST	1 3-BYTE CLOCK ADDRESS	1 INITIALIZE CLOCK
8195 AF	LXI H, CLKADR	1 RESET CLOCK	
8196 77	XRA A		
8197 23	MOV M, A		
	INX H		

Figure 1.1 - Continued

8198 77 8199 23 819A 77 819B C9	MOV M,A INX H MOV M,A RET				
819C F5 819D E5 819E 2A6280 81A1 23 81A2 226280 81A5 7C 81A6 B5 81A7 C2B181	J /ADW PUSH PSM PUSH H LHLD CLKADR INX H SHLD CLKADR MOV A,H ORA L JNZ CLKNXT		TRANSFER POINT FOR CLOCK INTERRUPT		COUNTS TIME THIS POINT IS REACHED ON INTERRUPT ONLY
81AA 3A6480 81AD 3C 81AE 326480	LDA CLKADR+2 INR A STA CLKADR+2				
81B4 3E70 81B3 D3DF 81B5 2A6080 81B8 7D 81B9 D3DD 81BB 7C 81BC D3DD 81BE 3E70 81C0 D3D7	CLKNXT MVI A,70H OUT OD7H LHLD INTRVL MOV A,L OUT ODDH MOV A,H OUT ODDH MVI A,08H OUT OD7H		RE-INITIALIZE TIMER 01 11 000 0 =1/256 SEC.		COUNTER-TIMER CHIP MUST BE RESET EACH TIME
81C2 3A6280 81C5 E60F 81C7 C2CF81 81CA 3EFF 81CC 326E80	LDA CLKADR ANI 0FH JNZ CLKNI MVI A,0FFH STA T16		INTERMPT CONTROLLER CALCULATE 1/16TH SEC INTERVAL		SET T16 TO FFH ON EVEN 16TH SEC.
81CF E1 81D0 F1 81D1 FB 81D2 C9	CLKNI POP H POP PSM EI RET		START CLOCK AGAIN		
81D3 F5 81D4 C5 81D5 D5 81D6 E5 81D7 DBCE 81D9 47 81DA 3E08	I6ADR PUSH PSM PUSH B PUSH D PUSH H IN OCEH MOV B,A MVI A,08H		RECEIVE LORAN DATA BURST INTERRUPT SAVE REGISTERS GET DATA BYTE RESET INTERRUPT CONTROLLER		STORES LORAN DATA IN BUFFER THIS POINT IS REACHED ON INTERRUPT ONLY

Figure 1.1 - Continued

81DC D3D/	OUT 0D/H	ENABLE INTERRUPTS	
81DE FB	LD S0SEQ	START OF SEQ ?	
81E2 B/	ORA A		
81E3 CA0982	JZ REGSED		
81E6 7B	MOV A,B	YES	
81E7 FEA	CPI 0AAH	BYTE 'AA' ?	FIRST BYTE OF VALID DATA
81E9 C23082	JNZ RDONE		STREAM IS AAH
81EC 216280	LXI H,CLKADR	TIME OF DAY	
81EF EB	XCHG		
81F0 216580	LXI H,ARRTIM	SAVE AS ARRIVAL TIME	ARRIVAL TIME IS SAVED
81F3 F3	DI	DISABLE INT (FREEZE CLOCK)	
81F4 1A	LDAX D		
81F5 77	MOV M,A		
81F6 13	INX D		
81F7 23	INX H		
81F8 1A	LDAX D		
81F9 77	MOV M,A		
81FA 13	INX D		
81FB 23	INX H		
81FC 1A	LDAX D		
81FD 77	MOV M,A		
81FE FB	EI	MOVE 3 BYTES	
		ENABLE INTERRUPTS	
81FF AF	XRA A		
8200 327180	STA S0SEQ		
8203 327280	STA POINTR		
8206 327380	STA DDONE		
8209 217090	LXI H,ARRAY		
820C 3A7280	LD POINTR	BUFFER	STORE BYTE IN BUFFER
820F 5F	MOV E,A	LOC IN BUFFER	
8210 AF	XRA A		
8211 57	MOV D,A	COMPUTE ADDR	
8212 19	DAD D	SAVE CHAR IN ARRAY	
8213 70	MOV M,B	INCREMENT POINTER	
8214 3A7280	LD POINTR		
8217 3C	INX A		
8218 327280	STA POINTR		
821B 47	MOV B,A		
821C 3A7480	LD PLIMIT	TEST AGAINST LIMIT	
821F 90	SUB B		
8220 C23082	JNZ RDONE	COMPLETE	
8223 3E01	VI A,01	SET 'DONE'	TELLS MAIN ROUTINE THAT ANOTHER
8225 327380	STA DDONE	SET 'START OF SEQUENCE'	UPDATE IS COMPLETE
8228 327180	STA S0SEQ		
822B 3E00	VI A,00H		
822D CD3870	CALL 0038H	RING BELL	(DISABLED)

Figure 1.1 - Continued

8230 E1	HDONE	POP H	RESTORE REGISTERS	
8231 D1		POP D		
8232 C1		POP B		
8233 F1		POP PSW		
8234 C9		RET		
8235 246280	TIME	LHLD CLKADR	WHAT TIME IS IT?	USED ONLY AS A DIAGNOSTIC
8236 AF		XRA A	LOW ORDER BYTES	FROM CRT TYPE GO 8043
8239 51		MOV D,A		
823A 3A6480		LDA CLKADR+2	HIGH ORDER BYTE	
823D 5F		MOV E,A	NON-MASK INTERRUPT LOC.	
823E C36600		JMP 0060H	TIME DISPLAYED IN DE,HL	
8241 217090	HDISP	LXI H,ARRAY	DISPLAY TDL-71J BUFFER IN HEX	USED ONLY AS A DIAGNOSTIC
8244 0E90		MVI C,9DH	157 BYTES	FROM CRT TYPE GO 8046
8246 CDD006	HL0XP	CALL 06D0H	157 BYTES	
8249 0610		MVI B,10H	16 BYTES PER LINE	
824B 7E	HL0XP1	MOV A,M		
824C CD1D03		CALL 031DH	HEX OUTPUT ROUTINE	
824F 3E20		MVI A,7	SPACE	
8251 CD4300		CALL 0043H	ROUT 1	
8254 23		INX H		
8257 0D		DCR C	ALL DONE	
8258 CA6082		JZ HL0XP2		
8259 05		DCR B	LINE DONE	
825A CA4682		JZ HL0XP		
825D C34882		JMP HL0XP1		
8260 CDD006	HL0XP2	CALL 06D0H		
8263 C9		RET		
8264 AF	MAIN	XRA A	MAIN PROGRAM LOOP	BEGIN MAIN PROGRAM
8265 327580		STA LASTMP	INITIALIZATIONS	CLEAR LAST WAYPOINT BYTE
8268 CDD006		CALL 06D0H	157 BYTES	CARRIAGE RETURN-LINE FEED TO CRT
826B CD7482	ML0XP	CALL TRACKR	TEST FOR NEW LORAN RECORD	TRACKR CHECKS FOR NEW LORAN DATA
826E CD2884		CALL DCALC	CALCULATE SMOOTHED OTW OUTPUT	DCALC UPDATES ANALOG OUTPUT
8271 C36882		JMP ML0XP		ITERATE
8274 3A7380	TRACKR	LDA DONE	NEW LORAN RECORD?	TRACKR ONLY HAS ACTIVITY WHEN A
8277 B7		ORA A		NEW LORAN DATA BURST IS RECEIVED
8278 C8		RZ	INIT NEW	

Figure 1.1 - Continued

8279 AF	XRA A	PROCESS EACH DATA BURST ONLY ONCE
827A 32/380	STA DUXINE	DISABLE INTERRUPTS
827D F3	DI	GET DECIMAL POINTS, DIST TO WP,
827E 210090	LXI H,ARRAY	TO-FR WAYPOINTS
8281 AF	XRA A	
8282 57	MOV D,A	
8283 1E09	MVI E,09H	
8285 19	DAD D	
8285 7E	MOV A,M	
8287 E608	ANI 08H	
8289 327/80	STA DECIML	
828C 23	INX H	
828D 46	MOV H,M	
828F 23	INX H	
8290 4E	MOV C,M	
8290 67	MOV H,B	
8291 69	MOV L,C	
8292 22/180	SHLD DTW	
8295 210090	LXI H,ARRAY	
8298 1E11	MVI E,11H	
829A 19	DAD D	
829B 7E	MOV A,M	
829C 32/680	STA WP	
829F FB	EI	
82A0 3A7/80	PRINT LORAN-C SOURCE DATA	
82A3 CD1D03	LDA DECIML	
82A6 3E20	CALL 031DH	
82A8 CD4300	MVI A,0	
82AB 2A7/880	CALL 0043H	
82AE 7C	LHLD DTW	
82AF CD1D03	MOV A,H	
82B2 7D	CALL 031DH	
82B3 CD1D03	MOV A,L	
82B6 3E20	CALL 031DH	
82B8 CD4300	MVI A,0	
82BB 3A7/680	CALL 0043H	
82BE CD1D03	LDA WP	
82C1 3E20	CALL 031DH	
82C3 CD4300	MVI A,0	
82C6 CD4300	CALL 0043H	
82C9 AF	XRA A	
82CA 32/180	STA VALID	
82CD 32/F80	STA NEWLEG	
82D0 3A7/80	LDA DECIML	
82D3 B7	ORA A	
		INVALIDITY TEST
		IF DECIMAL POINTS ARE LIT, OR
		IF CRT IS CONNECTED, THIS
		DATA WILL APPEAR
		RE-ENABLE INTERRUPTS
		NOTE FOUR DIGIT DTW WORD
		IF MASK BIT 3
		GET DECIMAL POINTS BYTE
		IF MASK ALL OTHER DEC. PTS. BIT
		SAVE IT
		DTW HIGH ORDER BYTE
		DTW LOW ORDER BYTE
		DISTANCE TO WAYPOINT 'DDD.D'
		WAYPOINTS
		TO/FR WAYPOINT NUMBERS 'DD'
		ENABLE INTERRUPTS
		WILL STAY UNSET IF TESTS FAIL
		TEST DECIMAL POINTS

Figure 1.1 - Continued

82D4 CA0383	JZ END1	TEST BLANK WAYPOINTS	
82D7 3A/680	LDA MP		IF ONE OR BOTH WAYPOINTS ARE BLANK, THEN DATA IS INVALID
82DA E6F0	ANI OFOH		
82DC FEFO	CPI OFOH		
82DE CA0383	JZ END1		
82F1 3A/680	LDA MP		
82E4 F6FF	ANI OFH		
82E6 F6FF	CPI OFH		
82E8 CA0383	JZ END1		
82EB 3E01	MVI A,01H		
82ED 32/A80	STA VALID		
82F0 3A/580	LDA LASTMP		
82F3 47	MOV B,A		
82F4 3A/680	LDA MP		
82F7 B8	CMP B		
82F8 CA0383	JZ END1		
82FB 32/580	STA LASTMP		
82FE 3E01	MVI A,01H		
8300 32/E80	STA NEWLEG		IF THIS MP PAIR <> LAST MP PAIR, THEN THIS IS A NEW LEG
8303 3A/A80	END1		
8306 B7	LDA VALID		
8307 C8	ORA A		
8308 3A/E80	RZ		NO FURTHER PROCESSING IF NOT VALID
8308 B7	LDA NEWLEG		
830C CA4383	ORA A		
830F CDE884	JZ UPDATE		
8312 210000	CALL SAVART		
8315 22/F80	LXI H,0000H		
8318 2A/880	SHLD DELT		
831E CDE85	LHLD DTM		
8321 2A8D80	SHLD BCD16		
8324 228780	CALL BCDCV		DTM IN BCD FORMAT CONVERT TO FIXED POINT BINARY RETURNS OUTJ6
8327 3A3180	LHLD OUT16		
832A 67	SHLD LASTDTM		
832B 2E70	LDA PROGSP		
832D 229780	MOV H,A		
8330 216C01	MVI L,00H		
8333 229980	SHLD A16		
8336 CD4A85	LXI H,016CH		
833C 228980	SHLD B16		
833F CDE86	CALL M1616		
8342 C9	LHLD OUT16		
	SHLD LASSPD		
	CALL PRINT		
	RET		
8343 116580	UPDATE	THIS ARRIVAL TIME	
	LXI D,ARRTIM		UPDATE ESTIMATED DISTANCE AND SPEED

Figure 1.1 - Continued

8346 216880	LXI H, ARRTIM*03H	LAST ARRIVAL TIME	!SUB24 CALCULATES DELTA ARR TIME
8349 016880	LXI F, ARRTIM*06H	!DELTA ARRIVAL TIME	!RESULT
834C C02585	CALL SUB24	!FIND TIME CHANGE	!SAVE TWO LOW-ORDER BYTES AS DELT
834F 2A6880	LHLD ARRTIM*06H	!SAVE DEL-TIME	!TEST FOR PASSAGE OF TIME > TLIM
8352 227F80	SHLD DELT	!ROUTINES TO TEST	
		!DATA CONTINUITY	
8355 016D80	LXI B, ARRTIM*08H	!HIGH ORDER BYTE ADDRESS	
8358 0A	LDAX B	!GET III-ORDER BYTE	
8359 B7	ORA A	!TIME LESS THAN 255 SEC	
835A CA6583	JZ UPJ	!DATA INVALID -- START OVER	
835D 3E01	MOV A, 01H	!PRESET MAX TIME LIMIT	
835F 327F80	STA NEWLEG	!DEL TIME (LOW ORDER 2 BYTES)	
8362 C30383	JMP ENDI	!COMPARE	
8365 2A8F80	UPJ	!CLEAR SIGN	!TEST FOR DISTANCE DELTA > 1 NMI
8368 EB	LHLD TLIM	!CONVERT BCD TO F.P.	
8369 2A7F80	XCHG		
836C C0D085	LHLD DELT	!CALC DELTA DIST	
836F FA5D83	CALL SUB16	!OUTPUT IN BC	
	JM TOLONG	!TAKE ABSOLUTE VALUE	
		!UNITS BYTE	
8372 AF	XRA A	!DELTA DIST > 1 MILE	
8373 32A380	STA SIGN	!20 MILES -- LIMIT ON DTM CALC	
8376 2A7880	LHLD DTM	!DTM	
8379 228880	SHLD BCD16	!>20 MILES	
837C C0FE85	CALL BCDCV	!RESET ARRIVAL TIME	
837F 2A8780	LHLD LASDTM	!ESTIMATE DTM	
8382 EB	XCHG	!ESTIMATE SPEED	
8383 2A8D80	LHLD OUT16		
8386 C0D085	CALL SUB16		
8389 60	MOV H, B		
838A 69	MOV L, C		
838D C0C685	CALL NEGST		
838F 7C	MOV A, H		
8391 B7	ORA A		
8392 C25D83	JNZ TOLONG		
8393 1614	MOVI D, 014H		
8395 1E00	MOVI E, 00H		
8397 2A8D80	LHLD OUT16		
839A C0D085	CALL SUB16		
839D FA5D83	JM TOLONG		
83A0 C0E884	CALL SAVART		
83A3 C0F884	CALL CDTM		
83A6 2A9F80	LHLD LASSPD		
83A9 2A9580	SHLD NXTSPD		

Figure 1.1 - Continued

83AC 2A/880	LHLD DTM	!CONVERT TO F.P. FORMAT	!CALCULATE 'DRIVE' WHICH IS FILTER
83AF 229780	CALL BCDV		!DRIVING FUNCTION (DIFFERENCE BETWEEN
83B2 CDM85	LHLD OUT16		!MEASURED DTM AND ESTIMATED DTM)
83B5 2A8080	XCHG		
83B8 EB	LHLD NXTDTM		
83B9 2A9380	CALL SUB16		
83BC CDM85	MOV H,B		
83BF 60	MOV L,C		
83C0 69	SHLD DRIVE	!FILTER DRIVER FUNCTION	
83C1 229180			
83C4 2A9D80	LHLD ALPHA1	!CALCULATE ALPHA, BETA	!GAINS ARE ELAPSED-TIME PROGRAMMED
83C7 229780	SHLD A16	!TIME-SENSITIVE GAIN	!CALCULATE DISTANCE GAIN
83CA 2A7F80	LHLD DELT		
83CD 229980	SHLD B16		
83D3 CDM85	CALL M1616		
83D3 2A8D80	LHLD OUT16		
83D6 EB	XCHG		
83D7 2A9880	LHLD ALPHA0		
83DA 19	DAD D		
83DB 229780	SHLD A16		!UPDATE DISTANCE ESTIMATE
83DE 2A9180	LHLD DRIVE		
83E1 229980	SHLD B16		
83E4 CDM85	CALL M1616		
83E7 2A9380	LHLD NXTDTM		
83EA EB	XCHG		
83EB 2A8D80	LHLD OUT16		
83EE 19	DAD D		
83EF 228780	SHLD LASDTM	!UPDATED FILTER	!SAVE REVISED ESTIMATE
83F2 2A1180	LHLD BETA1		
83F5 229780	SHLD A16		
83F8 2A7F80	LHLD DELT		!CALCULATE VELOCITY GAIN
83FB 229980	SHLD B16		
83FE CDM85	CALL M1616		
8401 2A8D80	LHLD OUT16		
8404 EB	XCHG		
8405 2A9F80	LHLD BETA0		
8408 19	DAD D		
8409 229780	SHLD A16		!UPDATE VELOCITY ESTIMATE
840C 2A9180	LHLD DRIVE		
840F 229980	SHLD B16		
8412 CDM85	CALL M1616		
8415 2A9580	LHLD NXTSPD		
8418 EB	XCHG		
8419 2A8D80	LHLD OUT16		
841C CDM85	CALL SUB16		

Figure 1.1 - Continued

841F 60	MOV H,B				
8420 69	MOV L,C				
8421 228980	SHLD LASSPD				
8424 C0FE86	CALL PRINT				
8427 C9	RET				
8428 DEE4	DCALC	IN OE4H			
842A 2F	CMA				
842B 328280	STA ANGLE				
842E 328F80	STA BCD16				
8431 AF	XRA A				
8432 328C80	STA BCD16+1				
8435 C0FE85	CALL BCDCV				
8438 2A8D80	LHLD OUT16				
843B 228380	SHLD ANGLEB				
843E 2A8380	LHLD ANGLEB				
8441 228780	SHLD A16				
8444 2A8580	LHLD ANGLE3				
8447 229980	SHLD B16				
844A C0A885	CALL M1616				
844D 2A8D80	LHLD OUT16				
8450 228380	SHLD ANGLEB				
8453 3A8E80	WAIT	LDA T16			
8456 B7		ORA A			
8457 C45384		JZ WAIT			
845A AF		XRA A			
845B 326F80		STA T16			
845E 327B80		STA FLAG			
8461 3A7A80		LDA VALID			
8464 B7		ORA A			
8465 CACE84		JZ SETFLG			
8468 3A7E80		LDA NEWLEG			
846B B7		ORA A			
846C C2CE94		JNZ SETFLG			
846F 116280		LXI D,CLKADR			
8472 216880		LXI H,ARRTIM+03H			
8475 016880		LXI B,ARRTIM+06H			
8478 C02585		CALL SUB24			
847B 2A8D80		LHLD ARRTIM+06H			
847E 227F80		SHLD DELT			
8481 7C		MOV A,H			
8482 FE08		CPI 08H			
8484 F8F884		JM CALCD			
8487 3F01	RESETI	MVI A,01H			
8489 327E80		STA NEWLEG			
848C C3CF84		JMP SETFLG			
			UPDATE FILTER		
				!SAVE REVISED ESTIMATE	
				!PRINT RESULTS ON CRT	
				!SUBROUTINE TRACKR FINISHED	
				!DCALC UPDATES ANALOG OUTPUTS	
				!DIGISWITCH SELECTS APPROACH ANGLE	
				!READ PORT A - DIGISWITCH ANGLE	
				!COMPLEMENT	
				!SET UP BCD16 FOR CONVERSION	
				!CONVERT TO 16-BIT BINARY F.P.	
				!BINARY VERSION OF ANGLE	
				!F.P. BINARY VERSION OF APPROACH ANGLE	
				!CONVERSION CONSTANT	
				!MULTIPLY	
				!SAVE CONVERTED ANGLE	
				!WAIT FOR T16 TO GIVE 1/16TH SEC INCR	
				!RESET IT	
				!LOAD FLAG BYTE 'INVALID'	
				!IF NOT VALID OR IF NEWLEG	
				!THEN DROP FLAG	
				!VALIDITY TESTS	
				!CURRENT CLOCK	
				!LASTOTM TIME	
				!DELTA TIME	
				!SAVE AS DELT	
				!TEST FOR TIME-OUT	
				!8 SECONDS	
				!SAVE TWO LEAST SIGNIFICANT BYTES	
				!FORCE A RESET IF >8 SECONDS	
				!SINCE LORAN-C UPDATE	

Figure 1.1 - Continued

849F CDF 884	CALCD	CALL CDTM	!CALCULATE CURRENT DTM AS NXDTM	!CALCULATE DTM FOR OUTPUT
8492 2A9380		LHLD NXTDTM	!TEST FOR DIST < 0.2 NM	!IF DTM < 0.2 MILES, STOP GUIDANCE
8495 EB		XCHG		
8496 213200		LXI H, 0032H		
8499 CDD85		CALL SUB16	!DROP FLAG	
849C F8784		JM RESET1		
849F 2A9380	CALCD1	LHLD NXTDTM	!CONVERSION FACTOR	!MULTIPLY DTM BY ANGLE
84A2 229780		SHLD A16	!MULTIPLY	!CONVERSION FACTOR
84A5 2A8380		LHLD ANGLE8		
84A8 229980		SHLD B16		
84AB CDA85		CALL M1616	!DIVIDE BY 16	!SCALE BACK BY 16
84AE 2A8D80		LHLD OUT16		
84B1 227C80		SHLD DTMC		
84B4 229780		SHLD A16		
84B7 2A6F80		LHLD PT10H		
84BA 229980		SHLD B16		
84BD CDA85		CALL M1616	!SAVE AS DTMC	
84C0 2A8D80		LHLD OUT16	!ANALOG BOARD OUTPUT	!OUTPUT ON ANALOG BOARD
84C3 227C80		SHLD DTMC		
84C6 220477		SHLD 7704H		
84C9 3EFF		MVI A, 0FFH		
84CB 327880		STA FLAG	!SET FLAG AS 'VALID'	!CALCULATE FLAG
84CE 210000	SETFLG	LXI H, 0000H		
84D1 3A7880		LDA FLAG	!FLAG VALID	
84D4 B7		ORA A		
84D5 C2D884		JNZ SET1		
84D8 213303	SET1	LXI H, 0333H	!FLAG INVALID	!OUTPUT ON ANALOG BOARD
84DB 220677		SHLD 7706H	!ANALOG BOARD FLAG OUTPUT	!SUBROUTINE 'DCALC' FINISHED
84DE C9		RET		
!***** END OF MAIN ROUTINE *****				
84DF 7D	SCA256	MOV A, L	!ROUTINE TO ROUND AND SCALE	!***** UTILITY ROUTINES FOLLOW *****
84E0 E680		ANI 080H	!DIVIDED BY 256	!SCA256 ROUNDS AND SCALES
84E2 B7		ADD A	!SHIFT TO CARRY BIT	!A 2-BYTE FIXED POINT WORD BY
84E3 8C		ADC H		!256 INTO A SINGLE BYTE (INT FUNCTION)
84E4 6F		MOV L, A		
84E5 2600		MVI H, 00H	!FRACTION IN HL	
84E7 C9		RET		
84E9 116580	SAVART	LXI D, ARRTIM	!ARRIVAL TIME ADDRESS	!SAVART MOVES ARRTIM INTO
84EB 216880		LXI H, ARRTIM+03H	!LAST ARRIVAL TIME	!LAST ARRIVAL TIME
84EE F3		DI	!FREEZE TIME VALUE	
84EF 1A		LDAX D		!INTERRUPTS DISABLED TO FREEZE TIME
84F0 77		MOV M, A		

Figure 1.1 - Continued

84F1 13	INX D				
84F2 23	INX H				
84F3 1A	LDAX D				
84F4 77	MOV M,A				
84F5 13	INX D				
84F6 23	INX H				
84F7 1A	LDAX D				
84F8 77	MOV M,A				
84F9 FB	RI				
84FA C9	RET				MOVE ARRTM TO LAST ARRTM IF TABLE INTERRUPTS
84FB 2AB280	CHITW				
84FC 222780	LHLD LASSPD				
8501 2A7080	SHLD A16				
8502 222280	LHLD DELT				
8503 222280	SHLD B16				
8504 222280	CALL M1616				
8505 2A3730	LHLD LASSPD				
8506 2A3730	CHITW				
8507 2A3730	LHLD OUT16				
8508 2A3730	CALL SCA256				
8509 2A3730	CALL SUB16				
8510 2A3730	MOV H,B				
8511 2A3730	MOV L,C				
8512 222380	SHLD NXTOTW				
8513 C9	RET				
8514 2A3730					
8515 2A3730					
8516 2A3730					
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8717 AF					
8718 AF					
8719 AF					
8720 AF					
8721 AF					
8722 AF					
8723 AF					
8724 AF					
8725 AF					
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8734 AF					
8735 AF					
8736 AF					
8737 AF					
8738 AF					
8739 AF					
8740 AF					
8741 AF					
8742 AF					
8743 AF					
8744 AF					
8745 AF					
8746 AF					
8747 AF					
8748 AF					
8749 AF					
8750 AF					
8751 AF					
8752 AF					
8753 AF					
8754 AF					
8755 AF					
8756 AF					
8757 AF					
8758 AF					
8759 AF					
8760 AF					
8761 AF					
8762 AF					
8763 AF					
8764 AF					
8765 AF					
8766 AF					
8767 AF					
8768 AF					
8769 AF					

```

8525 1A      LDAX D
8526 96      SUBH M
8527 02      STAX B
8528 21      INX H
8529 13      INX D
852A 13      INX B
852B 03      LDAX D
852C 1A      SUBH M
852D 96      STAX B
852E 02      INX H
852F 23      INX D
8530 13      INX B
8531 03      LDAX D
8532 1A      SUBH M
8533 96      STAX B
8534 02      RFI
8535 C9

```

```

      !LOAD A-LOW
      !SUBTRACT B-LOW FROM A-LOW
      !STORE IT IN C-LOW
      !INCREMENT THE REGISTERS

      !LOAD A-MID
      !SUBTRACT B-MID AND CARRY FROM A-MID
      !STORE IT IN C-MID
      !INCREMENT REGISTERS

      !LOAD A-HI
      !SUBTRACT B-HI AND CARRY FROM A-HI
      !STORE IT IN C-HI

```

```

      ! MULT8--AN 8-BIT MULTIPLICATION ROUTINE
      !
      ! THE MULT8 ROUTINE EFFECTS THE FOLLOWING: A X B = C
      ! A IS IN REGISTER A
      ! B IS IN REGISTER B
      ! D IS ASSUMED TO HAVE BEEN MADE ZERO BY THE CALLING ENTITY
      ! C IS THE 16-BIT RESULT IN HL

```

```

8536 0608    MULT8      MVI B,00H      !LOAD COUNTER
8537 1600    MVI D,00H
8538 210000   LXI H,00H
8539 1F      ROTAF3    RAR
853A D24285  JNC D      !ZERO OUT HL
853B 19      DAD D      !ROTATE A TO THE RIGHT
853C EB      XCHG      !NO ADD IF NON-CARRY
853D 29      DAD D      !ADD OE AND HL IN HL
853E 29      XCHG      !EXCHANGE DE AND HL
853F 05      DCR B      !HL=2XHL (SHIFT HL LEFT)
8540 C23DB5  JNZ ROTAF3 !EXCHANGE DE AND HL
8541 C9      RET       !DECREMENT COUNTER
                        !IF NOT ZERO YET, DO IT AGAIN
                        !DONE--RESULT IN HL

```

```

      ! M1616--A SUBROUTINE TO MULTIPLY TWO 16-BIT SIGNED FIXED-POINT NUMBERS
      !
      ! OUT -- RESULT16 = A16 * B16      OUT16= A16 * B16
      ! THIS ROUTINE MULTIPLIES TWO XX.XX NUMBERS TO GET A XX.XX NUMBER

```

```

854A 210000  M1616*    LXI H,0000H      !LEAST SIGNIFICANT BITS ARE LOST

```

Figure 1.1 - Continued

8540 220080	SHLD	OUT16	10CLEAR OUTPUT -- RESULT TOO LARGE FORCES OVERFLOW (C REGISTERS)
8551 113000	LXI	D,0000H	
8553 0E31	MVI	C,00H	10C=1 MEANS OVERFLOW
8555 AF	XRA	A	10SIGN SAVED
8556 32A380	STA	SIGN	
8559 2A9780	LHLD	A16	
855C C0C685	CALL	REGST	
855F 220780	SHLD	A16	10IF NEGATIVE, COMPLEMENT
8562 2A9980	LHLD	B16	
8565 C0C685	CALL	REGST	
8568 229980	SHLD	B16	
856B 3A9980	LDA	B16	10LOW B BYTE
856E 5F	MOV	E,A	
856F 3A9780	LDA	A16	10LOW A BYTE
8572 C03685	CALL	MULT8	
8575 7D	MOV	A,L	
8576 F687	ANI	080H	10ROUND-UP ROUTINE
8578 B7	ADD	A	10HIGH BIT OF LOW BYTE
8579 BC	ADC	H	10SHIFT INTO CARRY BIT
857A 320080	STA	OUT16	10ADD WITH CARRY
857D 3A9980	LDA	B16	10LOW OUT BYTE
8580 5F	MOV	E,A	10LOW B BYTE
8581 3A9980	LDA	A16+	10HIGH A BYTE
8584 C03685	CALL	MULT8	
8587 EH	XCHG	OUT16	10SWAP DE,HL
858A 2A8080	LHLD	D	10ADD TO OUT
858B 19	DAD	D	
858C 228080	SHLD	OUT16	
858F 3A9A80	LDA	B16+	10HIGH B BYTE
8592 5F	MOV	E,A	
8593 3A9780	LDA	A16	10LOW A BYTE
8595 C03685	CALL	MULT8	
8599 EB	XCHG	OUT16	
859A 2A8080	LHLD	D	
859B 19	DAD	D	
859E 228080	SHLD	OUT16	
85A1 3A9A80	LDA	B16+	10HIGH B BYTE
85A4 5F	MOV	E,A	
85A5 3A9880	LDA	A16+	10HIGH A BYTE
85A8 C03685	CALL	MULT8	
85AB 7C	MOV	A,H	
85AC B7	ORA	A	10OVERFLOW
85AD C0	RNZ	D,L	
85AE 55	MOV	A	
85AF AF	XRA	E,A	
85B0 5F	MOV	OUT16	
85B1 2A8080	LHLD	D	
85B4 19	DAD	D	
85B5 228080	SHLD	OUT16	
85B8 AF	XRA	A	

Figure 1.1 - Continued

85B9 4F	MOV	C,A	
85BA 3AA380	LDA	SIGN	
85BD B7	JRA	A	
85BE C8	RZ		! POSITIVE RESULT
85BF CD0785	CALL	COMPI6	! COMPLEMENT RESULT
85C2 228080	SRLD	OUT16	
85C5 C9	RET		! FINISHED !!

! REGIST--TEST FOR NEGATIVE 16-BIT F.P. VALUE & COMPLEMENT			
85C6 7C	! INPUT AND OUTPUT THROUGH HL		
85C7 E890	MOV	A,H	! TEST HIGH ORDER BIT
85C9 C8	ANI	080H	
85CA CD0785	RZ		! POSITIVE NUMBER
85CB 3AA380	CALL	COMPI6	! COMPLEMENT HL
85CD 3AA380	LDA	SIGN	
85DD 3C	INR	A	
85DE F601	ANI	01H	
85D3 32A380	STA	SIGN	! TRACK SIGN OF PRODUCT
85D6 C9	RET		

! 2'S COMPLEMENT OF HL			
85D7 7C	MOV	A,H	
85D8 2F	CMA		
85D9 67	MOV	H,A	
85DA 7D	MOV	A,L	
85DB 2F	CMA		
85DC C601	ADI	01H	! ADD 1
85DE 6F	MOV	L,A	! RESAVE
85DF 3E00	MVI	A,00H	! CLEAR A -- LEAVE CARRY BIT
85E1 8C	ADC	H	! CARRY INTO H
85E2 67	MOV	H,A	
85E3 C9	RET		

! CONVERT BCD DDD.D TO 16 BIT BINARY FLOATING POINT			
85E4 001A334D68C0C0V	! INPUT IS BCD16	! DDD.D	
85E9 809AB3CDE6	! OUTPUT IS OUT16	! XX.XX	
	DB	00H,01AH,033H,04DH,066H	! RESULT TOO LARGE OR NON-BCD DIGIT FORCES OVERFLOW (C REGISTER)
	DB	080H,09AH,0B3H,0CDH,0E6H	
85EE 210000	! CLEAR OUTPUT		
85F1 228080	LXI	H,0000H	
85F4 1600	SRLD	OUT16	
85F6 0E01	MVI	D,00H	! C=1 MEANS OVERFLOW
85F8 3AB880	MVI	C,01H	! LOW BCD BYTE
85FB E60F	LDA	BCD16	! MASK DECIMAL DIGIT
	ANI	0FH	

Figure 1.1 - Continued

85FD FE7A	CPI	0AH	!ILLEGAL CHARACTER
85FE F0	RP	H,B,DCNV	
8600 2FE485	LXI	E,A	
8603 5F	MOV	D	
8604 19	DAD	A,M	
8605 7E	MOV	OUT16	!FRACTIONAL BYTE
8606 32H090	STA	BCD16	!LOW ORDER BYTE
8609 3A4880	LDA	OF0H	!MASK UNITS DIGIT
8610 FE40	ANI		!SHIFT
860F 0F	RRC		
860E 0F	RRC		
8610 0F	RRC		
8611 0F	RRC		
8612 FE7A	CPI	0AH	!ILLEGAL CHARACTER
8614 F0	RP	OUT16+1	!HI ORDER BYTE
8615 32FE40	STA	BCD16+1	!HIGH BCD BYTE
8619 3A5C80	LDA	OFH	!TENS DIGIT
861B E60F	ANI	0AH	!ILLEGAL CHARACTER
861D FE7A	CPI		
861F F0	RP	E,A	
8620 5F	MOV	A,0AH	!MULTIPLY BY 10
8621 JE7A	MVI	MULT8	
8623 CD3685	CALL	OUT16+1	
8626 3A3E80	LDA	L	!HIGH BYTE
8629 85	ADD		!UNITS & TENS
862A D8	RC		!OVERFLOW
862B 32FE80	STA	OUT16+1	!HIGH BYTE
862E 3A3C80	LDA	BCD16+1	!HIGH BCD
8631 E6F0	ANI	OF0H	!MASK HUNDREDS
8633 0F	RRC		!SHIFT
8634 0F	RRC		
8635 0F	RRC		
8636 0F	RRC		
8637 FE7A	CPI	0AH	!ILLEGAL CHARACTER
8639 F0	RP		
863A 5F	MOV	E,A	
863B 3E64	MVI	A,064H	!MULTIPLY BY 100
863D CD3685	CALL	MULT8	
8640 7C	MOV	A,H	
8641 B7	ORA	A	
8642 C0	RNZ		!OVERFLOW
8643 3A3E80	LDA	OUT16+1	!HIGH BYTE
8646 85	ADD	L	!UNITS, TENS, HUNDREDS
8647 D3	RC		!OVERFLOW
8641 32FE80	STA	OUT16+1	!HIGH BYTE
864B AF	XRA	A	!O
864C 4F	MOV	C,A	!RESET ERROR FLAG
864D C9	RFT		!FINISHED !!

Figure 1.1 - Continued

864E F5	ROUTINE TO CONVERT HEX F.P. NUMBERS TO BCD DD.DD	
864F 7C	INPUT AND OUTPUT IN HL	
8650 CD8386	INPUT XX.XX	
8653 F1	OUTPUT DD.DD	
8654 F5	PUSH H	SAVE ARGUMENT
8655 2600	MOV A,H	CONVERT UNITS BYTE TO BCD
8657 29780	CALL BBCD	RESTORE ARGUMENT
865A 210064	POP H	SAVE UNITS BCD
865D 22980	PUSH A	CLEAR UNITS PART
8660 CD4A85	MVI H,00H	I=100 IN F.P.
8663 2AD80	SHLD A16	FRACTIONAL PART X100
8666 7D	LXI H,6400H	MASK HIGH BIT OF LOW BYTE
8667 E80	SHLD B16	SHIFT INTO CARRY BIT
8669 87	CALL M1616	ADD FRAC X100
866A 8C	LHLD OUT16	ROUND-OFF THE VALUE
	MOV A,L	I>99 ?
	ANI 080H	CARRY INTO UNITS DIGITS
	ADD A	CONVERT TO BCD
	ADC H	RECOVER UNITS DIGITS
	MVI B,00H	ADD CARRY BIT
8668 0600	CPI 064H	RESULT IN BCD
866D FE64	JM CVBCDI	14 BCD DIGITS IN HL
866F FA7386	INR 3	
8672 04	CALL BBCD	
8673 CD8386	MOV L,A	
8676 6F	POP A	
8677 F1	ADD B	
8678 80	DAA	
8679 27	MOV H,A	
867A 67	RET	
867B C9		

867C 09163248648BCD	ROUTINE TO CONVERT BYTE TO BCD DD	
	INPUT AND OUTPUT IN A	INPUT XX
	DB 07H,16H,32H,48H,64H,80H,96H	OUTPUT DD
8683 F5	PUSH A	SAVE ARGUMENT
8684 F670	ANI 0F0H	MASK HIGH ORDER NYBBLE
8685 0F	RRC	
8687 0F	RRC	
8688 0F	RRC	
8689 0F	RRC	SHIFT TO LOW POSITION
868A 21/C86	LXI H,BBCDT	
868D 5F	MOV E,A	
868E 1600	MVI D,00H	
8690 19	DAD D	LOAD ADDRESS IN TABLE
8691 F1	POP A	RESTORE ARGUMENT
8692 E60F	ANI 0FH	MASK LOW ORDER NYBBLE
8694 F80A	CPI 0AH	I>=10 ?

Figure 1.1 - Continued

8695 FA9886	JM HBCD1	IF 50, ADD 6 TO CONVERT TO BCD
8699 C606	ADI 06H	ADD HIGH NYBBLE IN BCD
869B 86	ADD M	RESULT IN BCD
869C 27	DAA	
869D C9	RET	
869E 2A8780	PRINT	ROUTINE TO PRINT RESULTS OF TRACKER UPDATE
86A1 C04F86		IF CRT IS ATTACHED, THIS DATA IS PRINTED
86A4 7D	LHLD LASPTW	DISTANCE TO WP
86A5 F5	CALL CVBCD	
86A6 7C	MOV A, L	
86A7 CD1D03	PUSH A	
86AA 3E2E	MOV A, H	HEX OUTPUT ROUTINE
86AC CD4300	CALL 031DH	
86AF F1	MVI A, 0	
86B0 CD1D03	CALL 0043H	
86B3 3E20	POP A	
86B5 CD4300	CALL 031DH	
	MVI A, 0	
	CALL 0043H	
86B9 2A8980	LHLD LASSPD	CURRENT GROUNDSPED ESTIMATE
86BB 229780	SHLD A16	
86BE 21100E	LXI H, 0E10H	3600/256 SCALES TO KNOTS
86C1 229980	SHLD B16	
86C4 CD4A85	CALL M1616	
86C7 0600	MVI B, 00H	
86C9 2A8D80	LHLD OUT16	
86CC 7C	MOV A, H	
86CD FE64	CPI 064H	
86CF FAJ786	JM PRINT1	HUNDREDS DIGIT
86D2 0601	MVI B, 01H	
86D4 D664	SUI 064H	
86D6 67	MOV H, A	SUB 100 FROM VALUE
86D7 78	MOV A, B	
86D8 CD1D03	CALL 031DH	PRINT HUNDREDS PLACE
86DH CD4E86	CALL CVBCD	CONVERT TO BCD
86DE 7D	MOV A, L	
86DF F5	PUSH A	
86E0 7C	MOV A, H	
86E1 CD1D03	CALL 031DH	
86E4 3E2E	MVI A, 0	
86E6 CD4300	CALL 0043H	
86E9 F1	POP A	
86EA CD1D03	CALL 031DH	
86ED 3E20	MVI A, 0	
86EF CD4300	CALL 0043H	
86F2 3A8280	LDA ANGLE	

Figure 1.1 - Continued

DISPLAY DIGI-SWITCH ANGLE
ICR LF

CALL 031DH
CALL 06DDH
RET

86F5 CD1D03
86F8 CD1D06
86F8 C9

Figure 1.1 - Continued

- 3) Software Initializations 80DEH
 - Initialize second serial port (Port B) and its baud rate.
 - Initialize parallel port and read initial groundspeed estimate.
 - Patch appropriate interrupt addresses into the interrupt table.
 - Set up interrupt routines for the clock and the Loran-C data stream.
- 4) Clock Interrupt Handler Routine 819CH
- 5) Loran-C Interrupt Handler Routine 81D3H
 - Receive data and load into a buffer
- 6) Main Routine 8264H
(Described below)
- 7) Utility Routines 82DFH
 - Round and scale
 - Save arrival time
 - Compute DTW
 - 16 bit subtract
 - 24 bit subtract
 - 8 bit multiply
 - 16 bit sign test & complement
 - Convert BCD to binary
 - Convert binary to BCD

The main routine consists of two major subroutines. The first, TRACKR (8274H), is the heart of the system. Its function is to update the tracking algorithm when a new Loran-C data stream has been received. It also tests the validity of the incoming data and drops the DME valid flag when necessary. The other subroutine, DCALC (8428H), calculates DTW sixteen times per second and controls the D/A converter. A flow-chart showing the basic functions of the software package appears as Figure 1.2.

The TRACKR subroutine updates the DTW and groundspeed estimates (using the equations in Section 1.4). It also examines the Loran-C

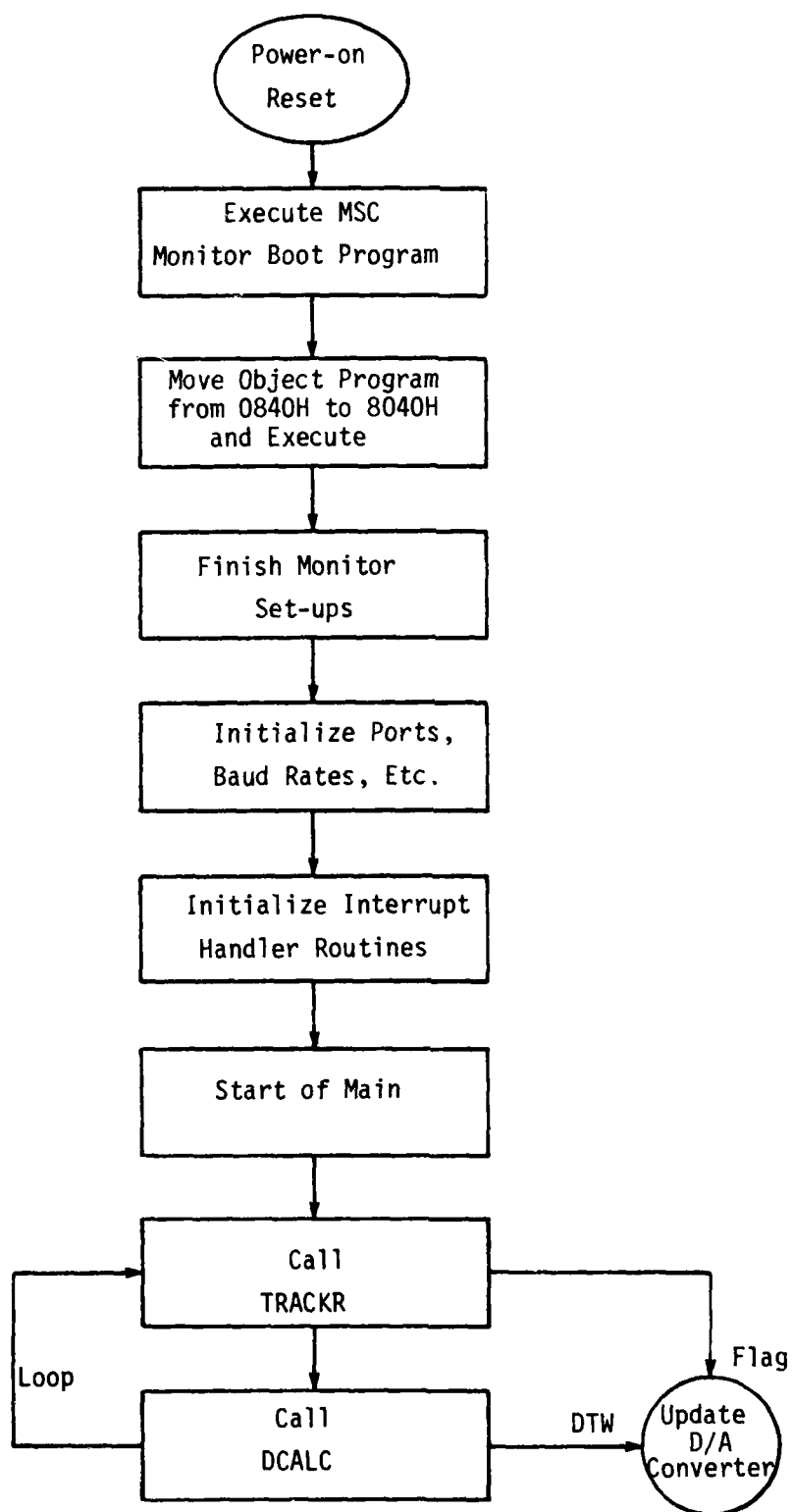


Figure 1.2 Overall Program Flow

data stream for determination of data validity and continuity. When data is invalid or discontinuous the DME valid flag is dropped. This subroutine performs an initialization function if one of several criteria are met: The waypoint pair is changed, the time since last update is greater than 16 sec, the change in Loran-C DTW exceeds one mile, or the DTW value itself exceeds 20 miles (indicating that an instrument approach is not in progress). A flow chart for the TRACKR subroutine appears as Figure 1.3.

The DCALC subroutine calculates current DTW estimate. This estimate is scaled by a factor derived from the pilot's approach angle selector. Any approach angle up to 9.9° may be selected. The flow chart for this subroutine appears as Figure 1.4.

1.6 SYSTEM TEST

Hardware and software checkout was performed on the bench using another computer system as a TDL-711 data stream simulator. System performance was evaluated over a broad range of off-nominal operating conditions including:

- 1) Velocity estimate wrong by ± 30 kts.
- 2) Data update delays ranging from 1 to 6 seconds.
- 3) Loran-C DTW random error magnitudes up to 0.1 nm (10).
- 4) Various Loran-C interruptions and failure modes.

Final system checkout was performed by installing the system in the Beech Queen Air operated by this company for navigation system test purposes. The complete system (TDL-711, Interface Unit, IDC VNAV, IDC Altimeter and approach angle selector) was installed in a normal operational configuration. The system was test flown on three different occasions. Approaches using the Loran-C/VNAV combination were conducted at Palm Beach International, Pahokee/Palm Beach Glades, and Sarasota-Bradenton airports. In all tests the guidance information was quite smooth and accurate (given the basic limitations of the Loran-C system). Approaches up to 7° were flown.

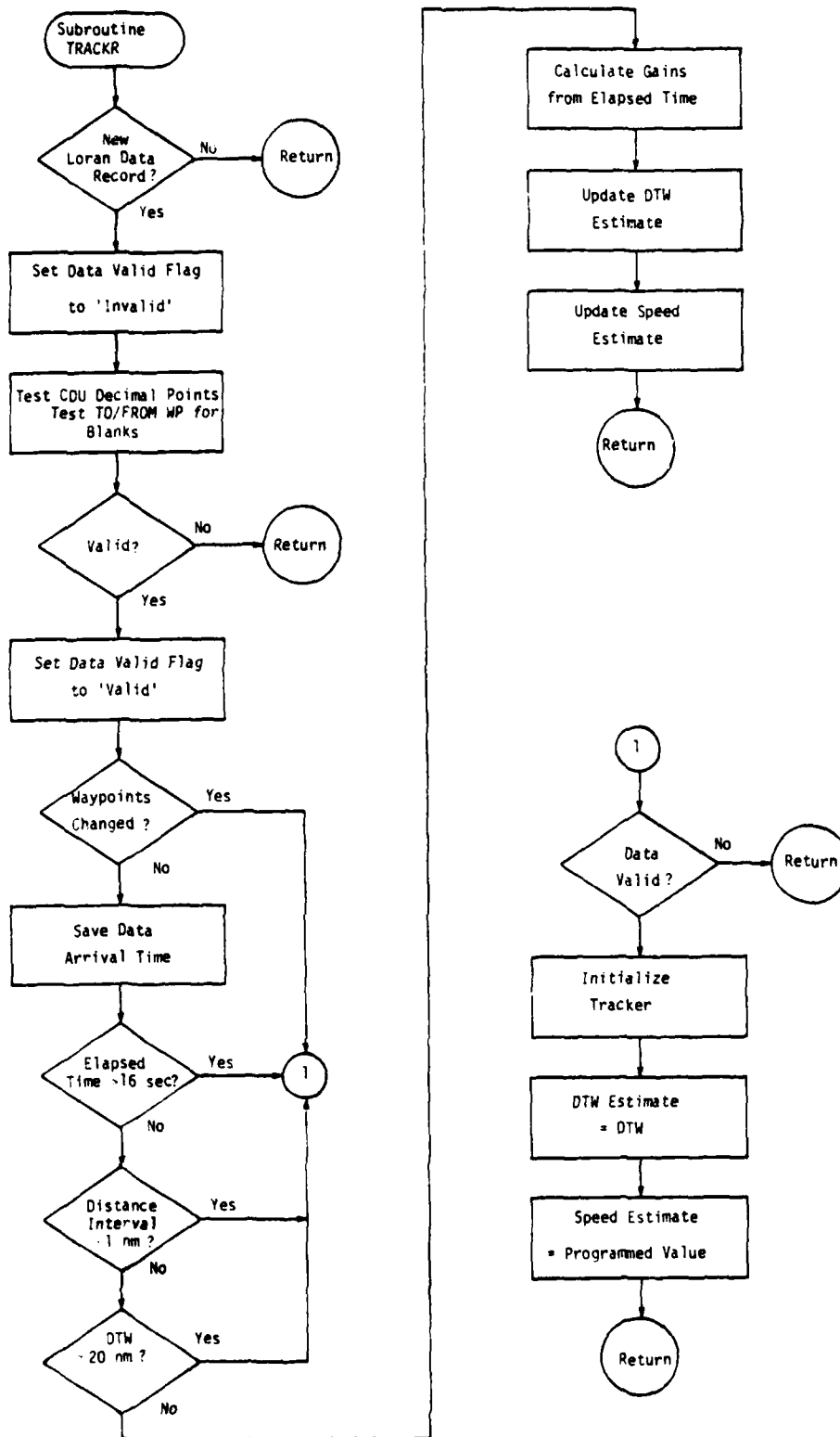


Figure 1.3 Subroutine TRACKR

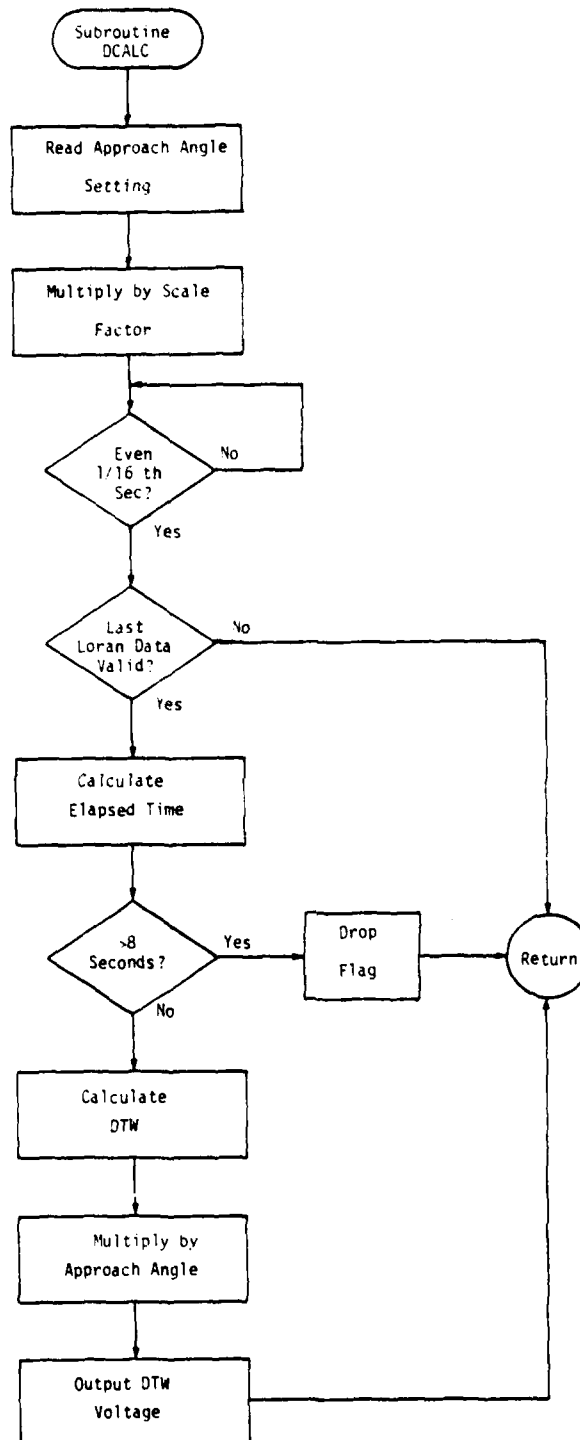


Figure 1.4 Subroutine DCALC

Introduction

The main purpose of the 3D Loran-C navigator is to provide let-down guidance for an equipped helicopter on a Loran-C non-precision approach. This hardware description describes the materials necessary to fabricate a proof-of-concept "bread board" demonstration unit to provide let-down guidance in a Loran-C environment. The unit is interfaced with a TDL-711 Loran-C navigator, an IDC VNAV system and a barometric altimeter. Certain factors that were addressed during this project are as follows:

- TDL-711 Loran-C navigator distance-to-go input
- Barometric altitude input
- Input data rates and filter requirements
- Output displayed on 2 each 1000 ϕ CDI's
- Validation/flag for guidance signal
- Helicopter speeds down to 20 kts
- Descent angles of 3 to 9 degrees with 6° nominal
- The expected performance envelope

Figure 2.1 shows a block diagram for the 3D Loran-C navigator. The system has been divided into three major areas: test equipment, the 3D Loran-C navigator and aircraft equipment. The figure shows how each component from the three major areas interacts with the other components in the system. Each component played a key role in either the development/testing or actual operational use of the 3D Loran-C navigator.

Basically, the 3D Loran-C navigator was developed so that the entire system could be tested in a laboratory environment. As shown in Figure 2.1 a computer terminal and its accompanying computer were used to test and develop the navigator's software. The computer terminal was used for display purposes while the computer was configured to simulate the TDL-711 data stream.

Normally the VNAV Alert unit receives DME (distance) data from the aircraft's onboard DME receiver. It in turn, based on altitude information received from the altimeter, field elevation set on the VNAV Alert unit, and a predetermined glide path angle, computes a

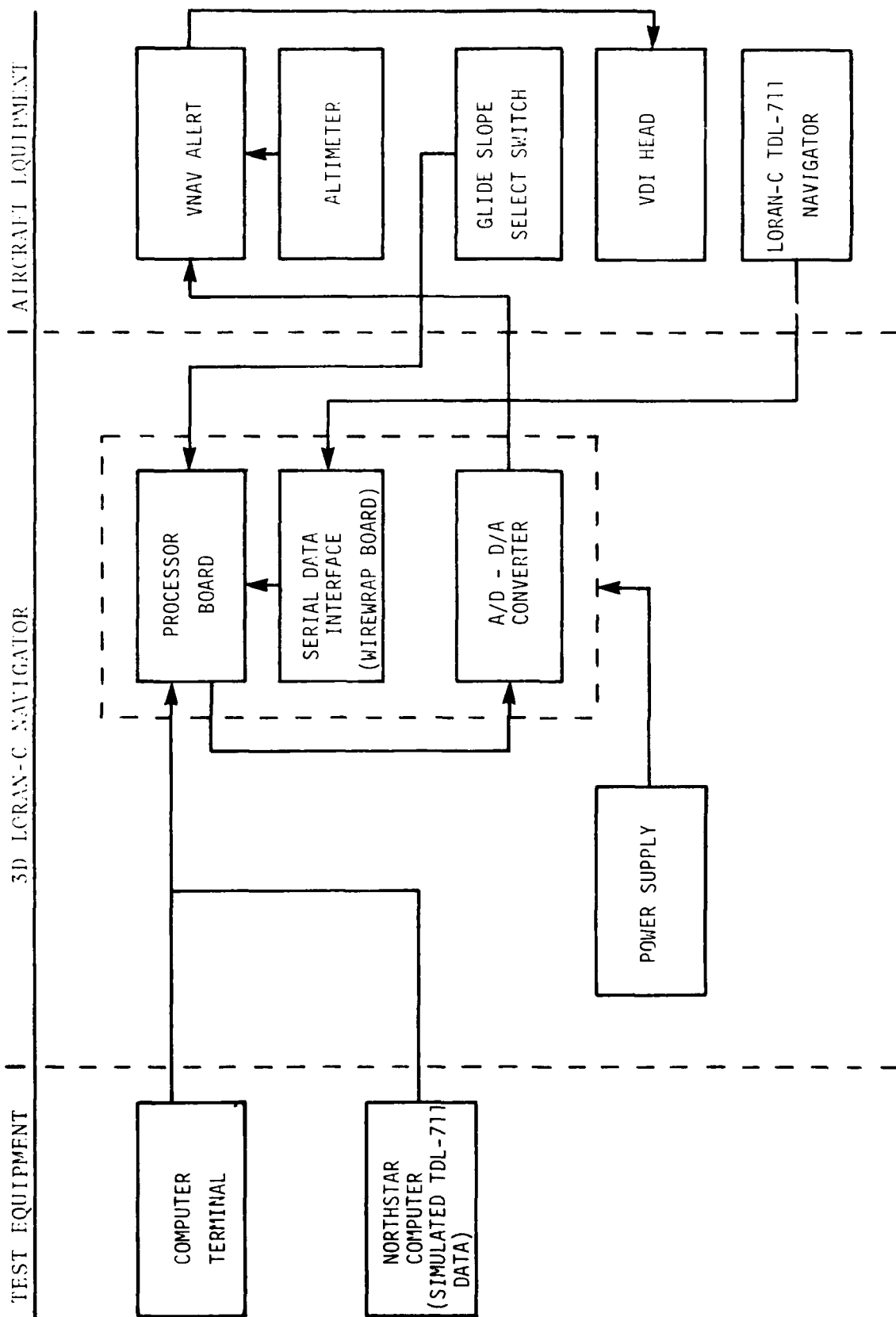


Figure 2.1 3D Loran-C Navigator Block Diagram

vertical deviation from the nominal 3 degree glide path and transmits this information to the VDI (vertical deviation indicator). For this particular operation, the following steps occur. The serial data interface receives DTW (distance to waypoint) information, along with various other necessary items, from the TDL-711 RPU and transmits the information to the processor board. The processor board smooths and filters the TDL-711 data (it is necessary to smooth the data because data is transmitted from the TDL-711 RPU at sporadic intervals, 1-6 sec) and also receives glide path angle data from the glideslope select switch. After certain computations are completed and this information is transmitted to the D/A converter, an analog distance voltage is sent to the VNAV Alert unit. From this point on, the system operates normally as discussed earlier in this paragraph.

The following sections describe the seven major components necessary to fabricate the 3D Loran-C navigator. Each component is described in detail along with the necessary interconnect descriptions and modifications necessary to make the unit function. The seven major components are as follows:

- MSC* 8201 Multibus Chassis
- MSC 8204 Universal Card
- MSC 8007 Z-80 Computer Board
- Burr-Brown D/A Converter Board
- Power Supply (DATEL $\pm 12V$ & $\pm 5V$)
- 3D Loran-C Chassis
- Aircraft Interconnect

2.1 MULTIBUS CHASSIS

The Multibus** Chassis used for the 3D Loran-C system was a Monolithic Systems Corp., MSC 8201. The chassis is multibus compatible and provides seven (7) slots for various computer card combinations. The MSC 8201 chassis is a standard RETMA rack mount, (i.e., 5.25" high, 19.00" wide and 8.50" deep). The chassis also offers a rigid .090" thick printed circuit backplane. Momentary rocker switches are provided for RESET and NMI (Non-Maskable Interrupt), with the RESET LED indicator being red and

/NOTE/ *MSC (Monolithic Systems Corporation)

**Registered Trade Mark of Intel Corporation

the NMI indicator being green [1].

The DC power connections ($\pm 12V$, $\pm 5V$, GND) were soldered directly into the backplane. Five (5) wires were required to make the appropriate connections into the backplane with a six (6) pin male Molex connector (Waldrom Part #1261 PRT) providing the connection from the DATEL PCT-12/2-5/6 power supply. Figure 2.2 shows how the Molex connector was wired as viewed into the male receptacle.

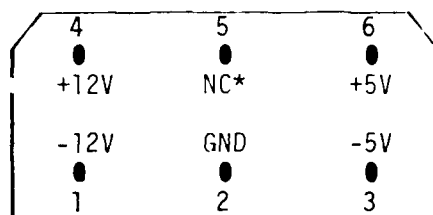


Figure 2.2 Multibus Power Connector

Table 2.1 presents the connector wire and its appropriate pin number (on the backplane) information.

Table 2.1 Multibus Backplane Power Supply Wiring

Backplane Pin#	Voltage
3/4	+5V
7/8	+12V
9/10	-5V
11/12	GND
79/80	-12V

Appendix A shows the "MCS 8201 Maintenance Manual Multibus Chassis". The appendix offers all of the added information, not mentioned above, necessary to operate the system.

/NOTE/ *NC - No Connection

2.2 WIREWRAP BOARD

The wirewrap board utilized for the 3D Loran C navigator was a Monolithic Systems Corporation, MSC 8204. The MSC 8204 Universal Card is for custom prototyping of Multibus* compatible systems. The MSC 8204 will hold a matrix of wirewrap sockets that accommodate any length components on width of 0.3, 0.4 and 0.6 inches. The MSC 8204 offers one, 26-pin I/O connector and two, 50-pin I/O connectors. The MSC 8204 accepts either a standard edge connector or the holes at the bottom of each conductive surface permit the mounting of a right-angle header connector. Power and ground planes terminate on uniformly-spaced pads for ease of access.

The MSC 8204 contains its own programmable, bus-master control system. Full address decoding permits the use of either memory mapped or normally isolated I/O addressing. Also, the MSC 8204 contains Transfer-Acknowledge logic and the option of including inhibits. See Appendix B for more detailed address bus, data bus, and control signals specifications.

The wirewrap board was used solely to interface the main computer board with the TDL-711 RDU data stream. Figure 2.3 shows the circuit diagram required to accomplish this task. The data interface required the use of one chip (DS 8820) (Appendix C) and several wirewrap connections on the MSC 8204 board. To accomplish this task, a 14 pin socket was installed at location D13 on the MSC 8204 board. After the chip (DS 8820) was installed, pins 1 and 3 were wirewrapped to pins 10 and 12 on the 26 pin connector, respectively. Pin 13 on the 26 pin connector was connected to ground on the MSC 8204 board. Pin 6, which is the output of chip DS 8820, is wirewrapped to pin 32 on the backplane connector of the board. This output (pin 6) is connected to the UART 8251 (RXD 3) chip on the main computer board. See the discussion of modifications made to the computer board in Section 2.3. As shown in Figure 2.3, two capacitors are required - a 0.01 μ f capacitor wired across pins 1 and 2, and a 100 pf capacitor wired across pin 5 and ground. Pin 4 on the DS 8820 is wirewrapped for +5 volts.

/NOTE/ *Registered Trade Mark of Intel Corporation

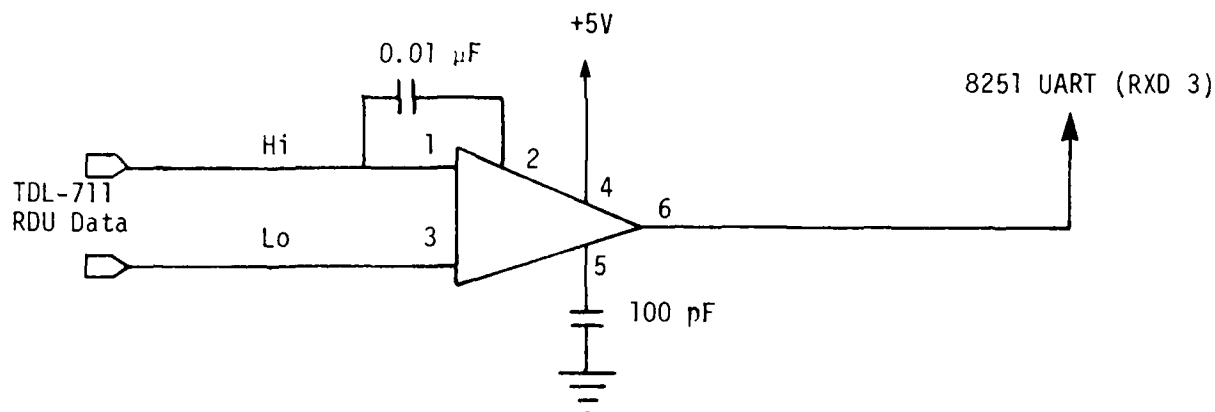


Figure 2.3 TDL-711 RDU Data Receiver [2]

2.3 MICROPROCESSOR BOARD

DESCRIPTION:

The microprocessor board used for the 3D Loran-C navigator was a Monolithic System Corporation MSC 8007. The Monolithic System Corporation MSC 8007 is a single-board OEM computer that is directly compatible with the industry standard MULTIBUS*. The 8080 software compatibility of the MSC 8007 provides an advanced, high-speed, next generation system designed to take full advantage of the Z80A** instruction set[3]. The Z80A microprocessor is fully compatible with the 8080A. The Z80A executes all 8080 instructions without modification.

SERIAL COMMUNICATIONS:

Three serial ports provide programmable interfaces that are synchronous or asynchronous. One port can be configured for either EIA RS-232-C, TTL or opto-isolated 20 mA loop signals. Two ports can be configured for EIA RS-232-C or TTL only. Signal specifications are:

Synchronous:

5- to 8-bit character; one or two programmable SYNC characters.

/NOTE/ *MULTIBUS is a registered trademark of Intel Corporation

**Z80A is a registered trademark of Zilog, Inc.

Asynchronous:

5- to 8-bit character; 1, 1-1/2, or 2 stop bits; choice of parity or error detection.

PARALLEL I/O:

One parallel, peripheral-interface controller (24 lines total) is used. All signals are both buffered and terminated on input and output configurations. Inverting and non-inverting transceivers are supplied.

INTERFACE SIGNAL:

MULTIBUS:

All signals conform with MULTIBUS specifications.

Parallel I/O:

All signals are TTL compatible.

Serial I/O:

Signals fulfill either EIA RS-232-C, TTL or 20 mA current loop convention depending on the MSC 8007 configuration.

Interrupt Requests:

All signals are TTL compatible.

Timer:

All signals are TTL compatible.

POWER REQUIREMENTS:

The MSC 8007 operates with MULTIBUS power supply voltages of +5V, -5V, +12V, and -12V.

PHYSICAL DIMENSIONS:

12 in. (Width) X 6.75 in. (Height) X 0.5 in. (Depth).

System options:

The MSC 8007 transmits and receives data either in parallel or serial form. Three serial I/O interfaces provide the MSC 8007 with serial data communication channels that are programmable and will operate either synchronously or asynchronously. Two of these serial

options were selected for the 3D Loran-C navigator. The serial I/O interfaces are designed around two software programmable devices - an 8251 USART and an 8253 Programmable Timer. The appropriate part numbers for the serial port options selected are as follows:

- 1) Serial I/O Kit 301-0072-002
- 2) Aux Serial I/O Kit 301-0072-004

The parallel I/O interface (Parallel I/O Kit 301-0072-003) (three, 8-bit I/O ports or two, 8 bit I/O ports with handshaking capabilities) provides a means of connecting the MSC 8007 to peripheral equipment that is designed to send and receive parallel data; in this particular case, the glide slope angle select switch. The 8255 Interface Controller receives and transmits the information as the 24 parallel lines of J1 (50 pin edge connector). There are three modes of operation available for the 8255. For this particular design, Mode 0 was selected which provides three separate 8-bit ports.

The MSC 8301 Uniform Monitor (Appendix E) was selected for the system and installed at location U101. The Uniform Monitor is a ROM resident stand alone I/O monitor. The program resides in 2K bytes of ROM and provides program loading, memory modification and similar basic functions. A second EPROM was also installed, containing the program developed for this system.

MODIFICATIONS PERFORMED TO MSC 8007 COMPUTER BOARD:

- 1) Jumper 117-118 is not implemented on this board. Its effect was duplicated by connecting Pin 9 to Pin 7 (ground) of the 74LS04 chip at position U5
- 2) Backplane pin 32 is connected to pin 8 of the socket for the MC1489 chip at location U9B. This connects the backplane pin 32 directly to the RXD input (pin 3) of the 8251 UART at position U19B. The 9th pin on the 1489 chip is removed from the socket.*
- 3) The optional Parallel I/O kit, Optional Serial I/O kit, and optional Auxillary Serial I/O kit have been installed.

/NOTE/ *For test purposes, the chip is installed with the 9th pin in place.

4) A second EPROM, containing the program developed for this system, is installed at position U102.

5) Jumper between pins 1 and 14 on the DIP header at position U6 connects output 0 of the CTC chip to the clock input of the aux. Serial port 1.

Jumper Selected Options:

With reference to Appendices A and B of the "User's Manual for MSC 8007", and the schematics in that manual, the following jumper options have been implemented. Where the option is a normal factory option, a (F) symbol appears. Where a factory option has been disconnected, a (F) symbol appears. The term N.C. means not connected.

Pin 1 to Pin 72 Pin 72 N.C. Pin 73 (F)	{	Disconnects the Backplane INT7/ from R0 of the interrupt controller, and connects Timer output 1 (implements real time clock)
Pin 48 to Pin 74 Pin 74 N.C. Pin 75 (F)	{	Disconnects the Backplane INT6/ from R2 of the interrupt controller, and connects RXRDY/ from Aux UART 1 (implements interrupt driven Loran-C data receiver)
Pin 11 to Pin 12		Implements U2 buffer chip to parallel port B as input mode. Allows use of port B to select Nominal Approach Speed.
Pin 18 to Pin 19		Implements U4 buffer chip to parallel port A as input mode. Allows use of port A for digiswitch selection of approach angle.
Pin 24 to Pin 27 Pin 24 to Pin 28	{	Selects 2 MHz clock line as driver for clocks 1 and 0 (respectively) of 8253 CTC.
Pin 29 to Pin 25 Pin 29 to Pin 26	{	Grounds the gates for clocks 0 and 1 (respectively) of the 8253 CTC (allows free-running operation)

Pin 40A to Pin 42A	Selects on-board clock for the Optional Serial port
Pin 40B to Pin 42B	On board clock, Aux Serial Port 1.
Pin 41B to Pin 42B	Implemented for test purposes.
Pin 43A to Pin 44A	{ Connects ± 12 volts to the 75188 driver chip at U10A
Pin 46A to Pin 47A	
Pin 43B to Pin 44B	{ Connects ± 12 volts to the 75188 driver chip at U10B
Pin 46B to Pin 47B	
Pin 50 to Pin 51(F)	Supplies 2 MHz to CTC
Pin 54 to Pin 55(F)	Not Used
Pin 58 to Pin 59(F)	Supplies 4 MHz to Z80
Pin 60 to Pin 61(F)	Connects Reset to Bus Reset
Pin 62 to Pin 63(F)	Connects 8 MHz to Bus
Pin 64 to Pin 65(F)	Implements Watchdog Timer
Pin 68 to Pin 69(F)	Connects 8 MHz to Bus
Pin 70 to Pin 71(F)	Connects NMI to Bus NMI
Pin 76 to Pin 77(F)	{ These connect backplane lines INT5/ through INT0/ to Interrupt controller lines R2 through R7, respectively
thru	
Pin 86 to Pin 87(F)	
Pins 88 through 95	
Factory Set	
Pins 96A to Pin 97A	Implements Serial Port DSR line
Pin 98A to Pin 99A	Makes TXC=RXC
Pin 96B to Pin 97B	As above for optional Aux
Pin 98B to Pin 99B	Serial Port 1
Pins 100 through 116	
Factory Set	

2.4 A/D - D/A MICROCOMPUTER SYSTEM

The A/D - D/A Microcomputer-compatible system used was a Burr-Brown model MP8418. This particular analog I/O system is electrically and mechanically compatible with and interfaced directly to Intel's Multibus and other microcomputers of similar configuration.^[4]

The analog input portion of the MP8418 includes: an analog multiplexer, resistor-programmed instrumentation amplifier or, a software-programmable amplifier (gain of 1 to 1024); sample/hold amplifier and a 12-bit A/D converter. An optional analog output system is included on the same board. It consists of two 12-bit D/A converters. The MP8418 is a 15-channel, differential or a 31-channel single-ended analog input system.

Table 2.2 presents the A/D - D/A board jumper configuration. Listed are the preset (factory) jumper configurations and the configuration as required to make the A/D - D/A board system compatible with the 3D Loran-C navigation system. Essentially only two areas require a modification from the factory configuration; these are the address jumpers and the analog output jumpers. Concerning the address jumpers, it is only necessary to change the sense of the bit on ADR F. This is accomplished by removing jumper 57 and installing jumper 65.

The Burr-Brown analog board is normally factory set to provide a $\pm 10V$ output on each digital-analog controller (DAC) with two's complement coding (jumpers 23, 25, 19, 28 and 46). As Table 2.2 indicates, certain modifications were made so that an output of 0V to +5V was available at both the DAC1 and DAC2. In addition, it was necessary to change from two's complement coding to straight binary. All of this was accomplished by removing jumpers 23, 25, 19, 28, 46 and replacing them with jumpers 22, 24, 26, 18, 20, 27 and 47. Also, the gain and the offset had to be adjusted for DAC2 so that the proper voltage tolerance could be obtained.

Appendix F presents the factory manual for the Burr-Brown A/D - D/A Converter. Any additional information or clarification necessary can be obtained from Appendix F.

Table 2.2 A/D - D/A Microcomputer Jumper Configuration

	Factory	Present Configuration	Modification
Address Jumpers	34 32 35 50 51 52 61 54 55 56 57	34 32 35 50 51 52 61 54 55 56 - 65	Remove Add
ADRF			
Analog Output { DAC1 { +10V { DAC2 { 2's complement code Output & Feedback Lines DAC1 DAC2 0 to +5V { DAC1 { DAC2 { Straight Binary	23 25 19 28 46 79 21 22 24 26 18 20 27 47	- - - - - 79 21 22 24 26 18 20 27 47	Remove Remove Remove Remove Remove Add Add Add Add Add Add Add
A/D Converter Range ±10V { Setting { 2's complement mode {	12 14 49 69	12 14 49 69	

Table 2.2 A/D - D/A Microcomputer Jumper Configuration (continued)

	Factory	Present Configuration	Modification
15 Channel Differential	3 4 7 42	3 4 7 42	
Grounds CH0 Input	80	80	
Halt Mode	17 29 30 81	17 29 30 81	
Interrupt Vector (Int.1)	71	71	
Optional Expander Board	39 43	39 43	

2.5 POWER SUPPLY

The power supply used for the 3D Loran C navigation system was a DATEL INTERSIL, PCT-12/2 - 5/6. The system utilizes an input line voltage of 115 VAC and has output voltages of ± 12 VDC and +5 VDC.

The specifications for the DATEL power supply are as follows:

Input Voltage*	115/230VAC $\pm 10\%$
Line Frequency	48-440 Hz
Output Voltage Adjustment	$\pm 10\%$
Output Ripple	2mV RMS, max.
Transient Response	50 μ sec. max.
Output Protection	Current Limiting or Foldback Limiting
Isolation Resistance	100 Meg. min.
Voltage Stability, after warmup	$\pm 0.25\%$, 24 hours
Isolation Capacitance	250pF max.
Breakdown Voltage	1500VAC min.
Operating Temperature Range	0°C to 50°C (No Derating)
Storage Temperature Range**	-25°C to +85°C
Output Voltage	± 12 V @ 2A/5V @ 6A
Chassis Size (in.)	11.25 x 4.87 x 2.75
Weight (lbs)	5.8

One minor modification had to be made so that a -5V power source could be obtained from the DATEL power supply. By utilizing a -5V regulator and two polarized filter capacitors, the task was

/NOTE/ *Input voltage is selected by transformer connection

**Derated to 40% of output current at 71°C.

accomplished easily. A solder terminal strip was mounted directly to the DATEL chassis so that all of the necessary connections could be made. Figure 2.4 shows the wiring schematic and general assembly for the -5V power source.

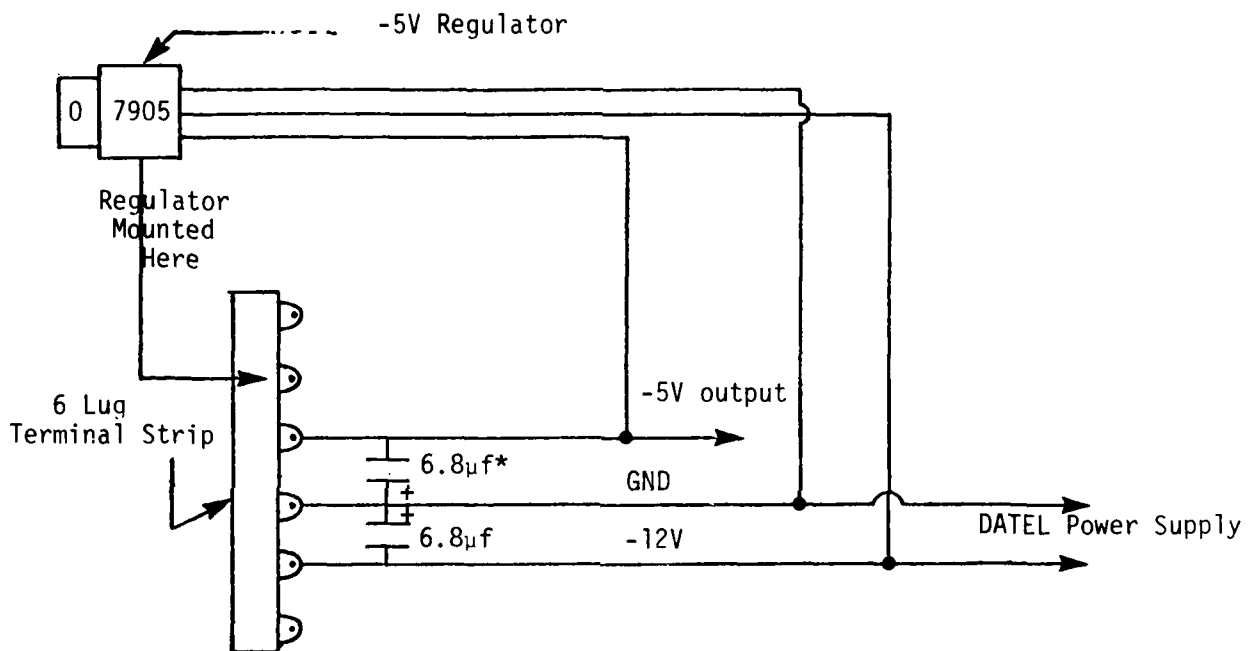


Figure 2.4 -5V Power Source

All of the wires from the power supply terminate into a 6 pin female MOLEX connector. Figure 2.2 of the Multibus chassis section presents the pin configuration for power connector. The 115VAC input is wired to the transformer on the power supply as per the instructions.

/NOTE/ * $\pm 20\%$ tolerance, tantalum capacitors

2.6 3D LORAN-C CHASSIS

Description:

The 3D Loran-C chassis is composed entirely of the components described previously in Sections 2.1 through 2.5. All of the components are securely fastened to a piece of .080 aluminum plate that measures 17.75 inches by 14.75 inches. All of the components are fastened to the plate using standard 10-32 aircraft bolts with elastic-stop nuts. Aircraft mounting is accomplished by utilizing a standard 19 inch electronics rack. This is easily accomplished since the Multibus chassis is a standard 19 inch RETMA rack mount. Figure 2.5 shows a bottom view of the 3D Loran-C chassis. As shown in the figure, the chassis itself is composed of four major components. They are: the Multibus chassis, the DATEL power supply, barrier strip and the power connector with fuse.

Chassis Power:

The 3D Loran-C chassis operates on 115 VAC power, either at 60 Hz or 400 Hz. The power connection is made at the chassis using a male 3 pin Cannon plug (MS 3057-6A), rated at six (6) amperes. Figure 2.6 shows the power schematic for the 3D Loran-C chassis. 20 AWG wire was more than sufficient for this installation.

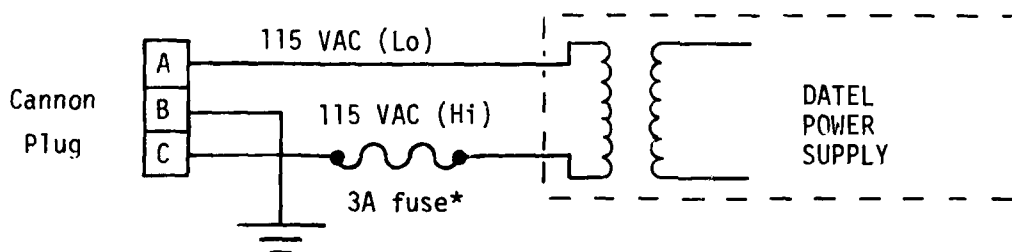


Figure 2.6 3D Loran-C Power Schematic

/NOTE/ *Standard chassis mount 3A fuse.

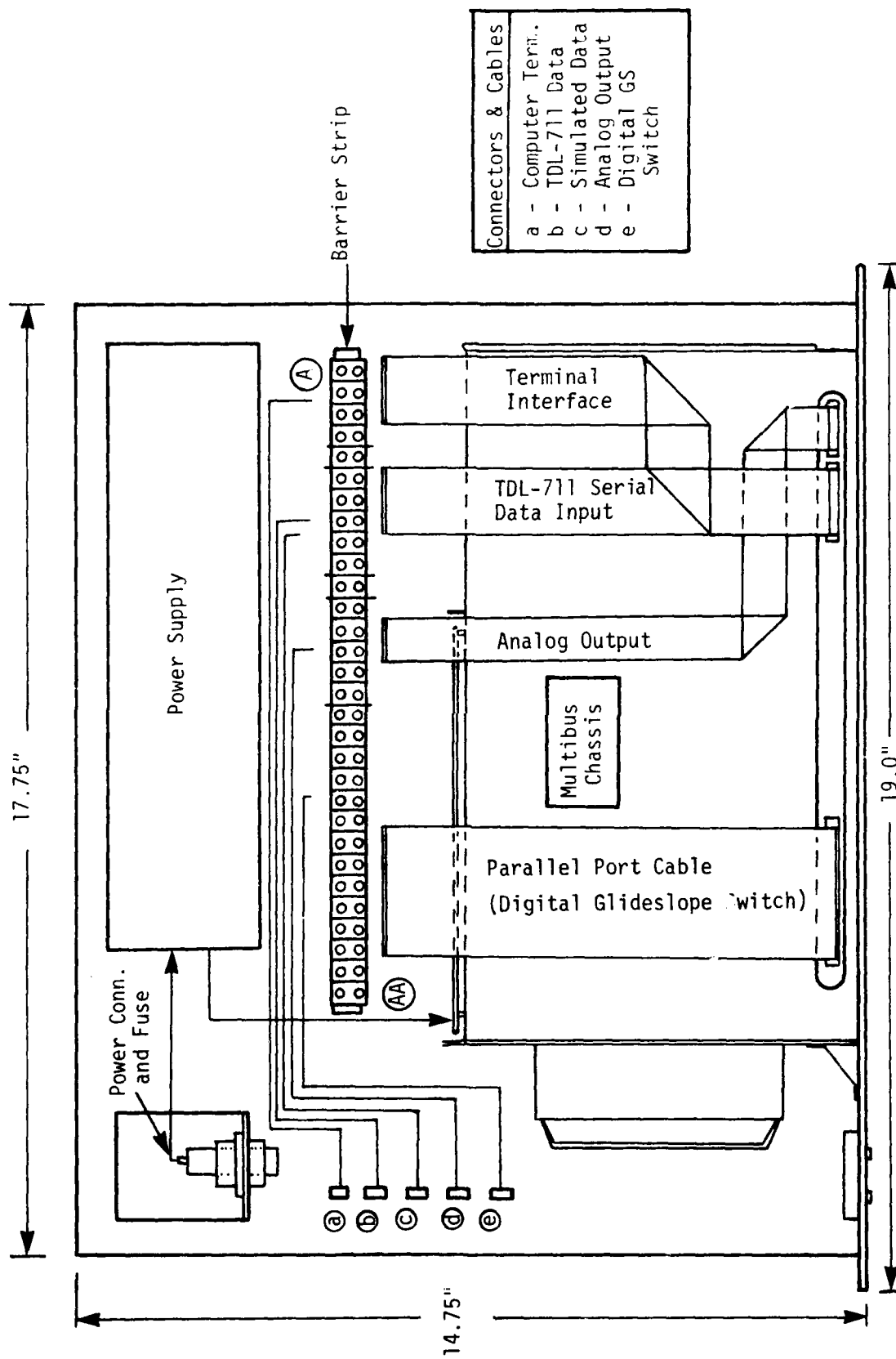


Figure 2.5 3D Loran-C Chassis

Chassis Interconnection:

Figure 2.7 presents a detailed wiring schematic for the 3D Loran-C chassis. A 30 lug barrier strip was utilized to make interconnection between peripheral devices and chassis components. Interconnection between the wirewrap board (MSC 8204), in addition to serial port 1 on the processor board, was made using a 26 conductor ribbon cable. Similarly, a 50 conductor ribbon cable was utilized for the interconnection between the processor board's parallel port and the barrier strip. Likewise, the A/D - D/A converter required a 20 conductor ribbon cable to make the appropriate connections. All of these ribbon cables are securely fastened to the Multibus chassis using two bolts and a flat aluminum plate. Those connections indicated in the dashed boxes are for testing and prototype development purposes only. For normal operation, these connections would not be made. Most of the connections made on the peripheral side of the barrier strip are made with 4 and 12 pin Molex connectors (see Figure 2.8 for the appropriate part numbers). Wiring for these connections was accomplished using standard 24 AWG wire.

As shown in the lower lefthand corner of Figure 2.7, a small modification was necessary to supply the appropriate flar voltage to the VNAV Alert unit. The circuit is a very simple transistor-resistor network utilizing a standard NPN Silicon (2N2484) transistor. The circuit is activated through the A/D board output signal [0V (Hi), 2V (Lo)]. When activated, 18VDC is transmitted to the VNAV Alert unit.

Test/Operational Configuration:

Several items on the 3D Loran-C chassis must be either connected or disconnected to make the transition from test to operational configuration. As mentioned earlier, on Figure 2.7 those items utilized for testing purposes only are indicated by the dashed boxes. Basically, to operate the 3D Loran-C in the test mode, the following operations must be completed.

- 1) Connect pins 8 & 9 on the processor board parallel port connector. (A plug is provided on the ribbon cable for this purpose.) This selects 4800 baud rather than 20833 baud used for the TDL-711.

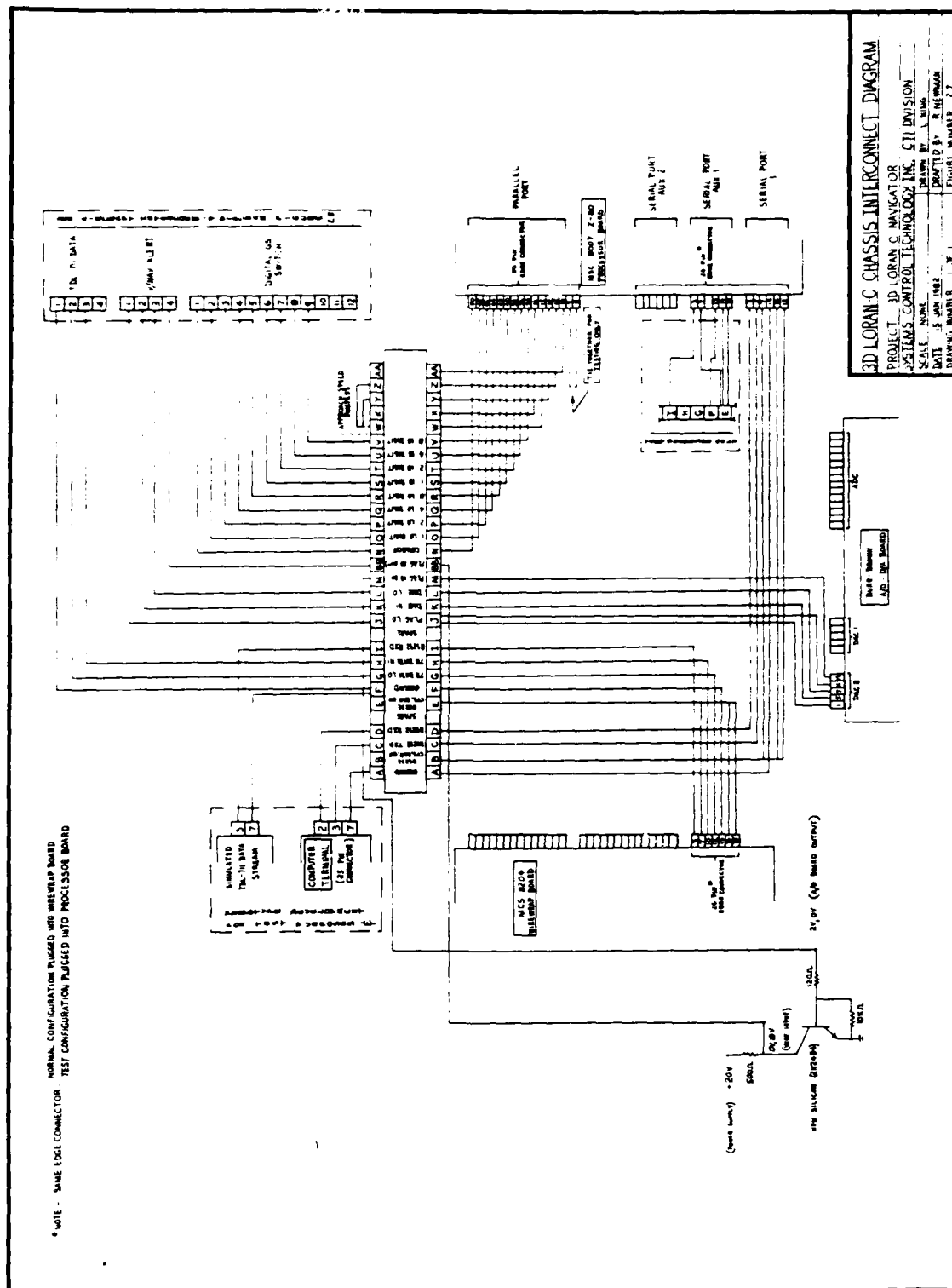


Figure 2.7 3D Loran-C Chassis Instrument Diagram

- 2) Remove the wirewrap board and connect the 26 pin edge connector normally plugged into the wirewrap board into aux serial port 1. (Plug J3)
- 3) Connect the computer terminal plug and the simulated TDL-711 data stream plug to their respective devices.
- 4) Insert the 9th pin on the MC1489 chip at location U9B on the processor board. (Substitute a normal 1489 chip)

To operate the 3D Loran-C navigator in its normal mode of operation, the following conditions must be checked.

- 1) Disconnect pin 8 & 9 on the processor board parallel port.
- 2) Insert the wirewrap board, and plug in the Loran data stream 26 pin edge connector.
- 3) Disconnect and secure all external computer plugs.
- 4) Remove the 9th pin on the MC1489 chip at location U9B on the processor board.

2.7 AIRCRAFT INTERCONNECTION

The 3D Loran-C navigator unit is connected to three major components in the aircraft. They are the TDL-711 RPU, Intercontinental Dynamics V/NAV ALERT (541-24912-112) unit and the digital GS switch (AMP 8012). The 3D Loran-C receives distance to the waypoint information from the TDL-711 RPU where it is in turn filtered, smoothed and converted to an analog output signal. This analog output signal is transmitted directly to the V/NAV ALERT unit. The 3D Loran-C navigator itself operates on 115 VAC power supplied by the static inverter onboard the aircraft. Glide path descent angle information is supplied to the 3D Loran-C navigator by a digital switch mounted on the aircraft's instrument panel. Figure 2.8 shows the 3D Loran-C navigator interconnection diagram.

Figure 2.9 shows the interconnection between the V/NAV ALERT unit, the altimeter and the glideslope indicator. The diagram is self-explanatory.

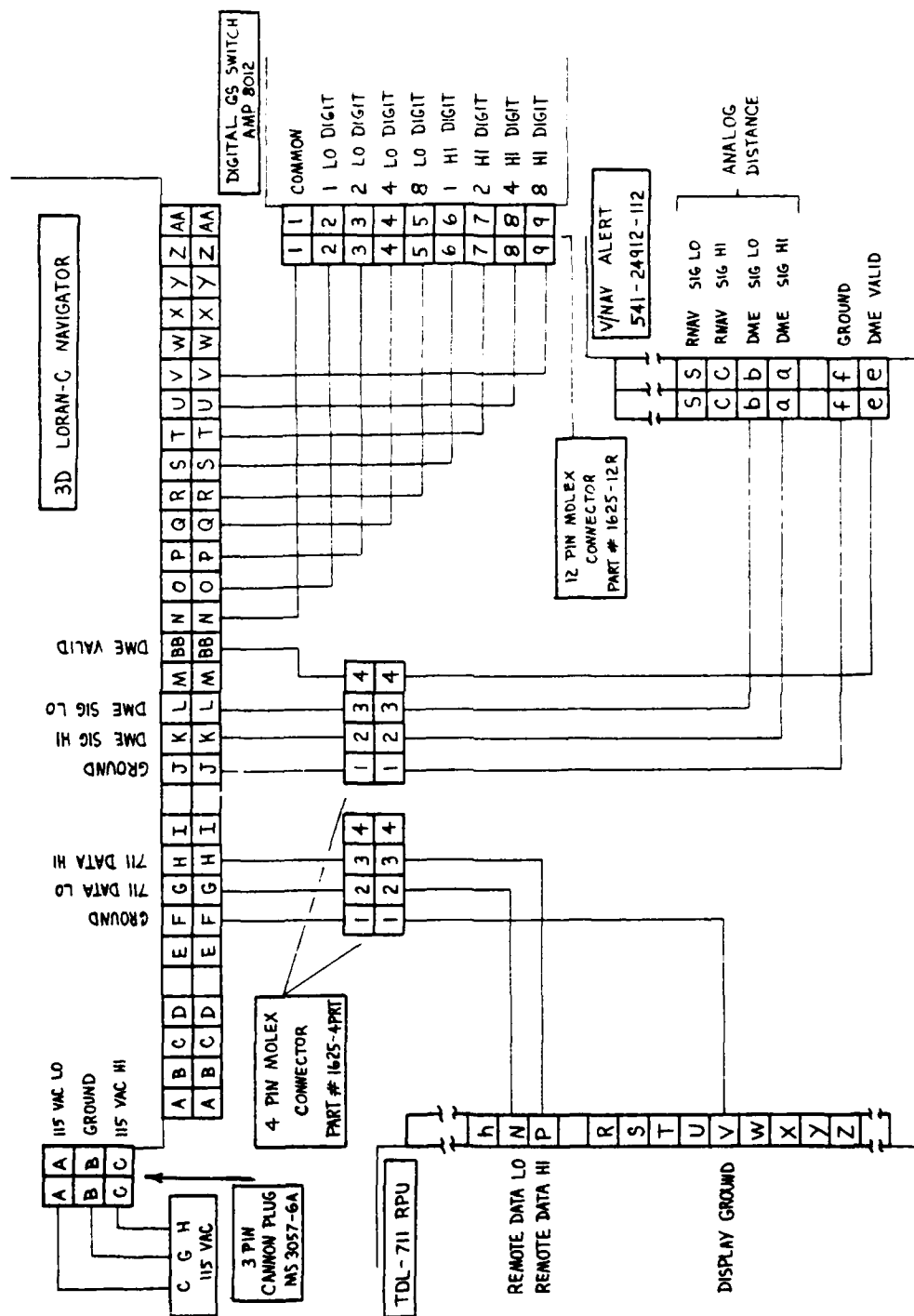
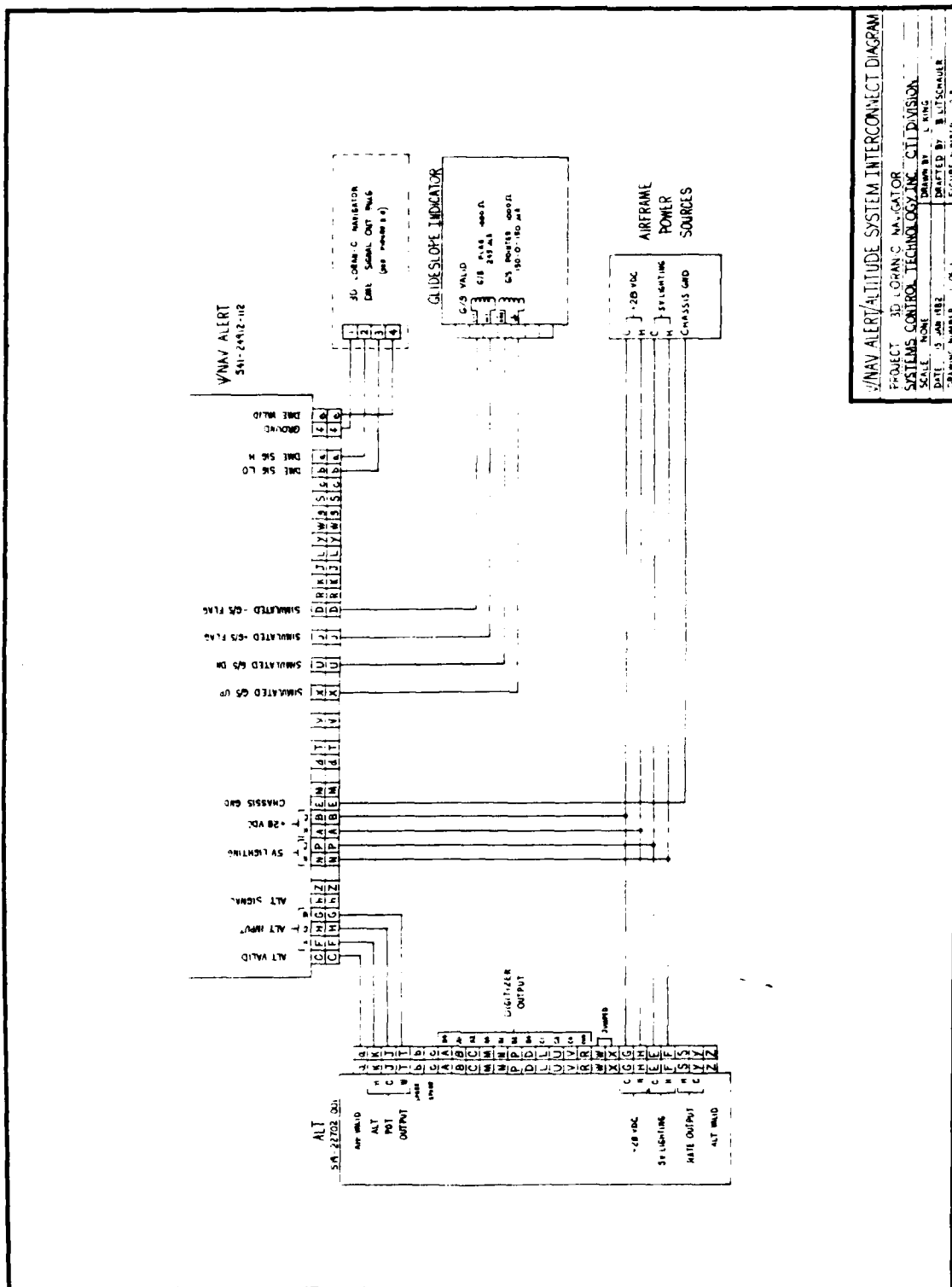


Figure 2.8 3D Loran-C Navigator Aircraft Interconnect Diagram



VNAV ALERT/ALTITUDE SYSTEM INTERCONNECT DIAGRAM
 PROJECT 3D LOGIC NAVIGATOR
 SYSTEMS CONTROL TECHNOLOGY INC. CIT DIVISION
 SCALE NONE
 DATE 13 JAN 1982
 DRAWING NUMBER 1 OF 1
 DESIGNED BY E. LUTSCHER
 FIGURE NUMBER 2.9

Figure 2.9 VNAV Alert/Altitude System Interconnect Diagram

REFERENCES

1. Anonymous, "MSC 8201 Maintenance Manual Multibus Chassis", Monolithic Systems Corp., 1978.
2. Anonymous, "TDL-711 Interface CICTS", Sierra Nevada Corp., (Circuit Diagram), January 8, 1981.
3. Anonymous, "User's Manual For MSC 8007", Monolithic Systems Corp., 1980.
4. Anonymous, "Microcomputer Analog I/O Systems", MP8418, Burr-Brown Research Corporation, 1978.
5. T.E. Scalise, E.H. Bolz, and E.D. McConkey, "West Coast Loran-C Flight Test", Systems Control, Inc. (Vt.), Champlain Technology Industries Division for the Federal Aviation Administration Systems Research and Development Service, FAA-RD-80-28, March 1980.

APPENDICES

- APPENDIX A -- "MSC 8201 Maintenance Manual Multibus Chassis",
Monolithic Systems Corp., 1978. (Included by Reference).
- APPENDIX B -- "Maintenance Manual For Universal Card MSC 8204",
Monolithic Systems Corp., 1978. (Included by Reference).
- APPENDIX C -- "DS7820A/DS8820A Dual Line Receiver", National Semiconductor
Corp. Also "TDL-711 Interface CICTS", Sierra Nevada Corp.,
(Circuit Diagram), January 8, 1981. (Included by
Reference).
- APPENDIX D -- "User's Manual For MSC 8007", Monolithic Systems Corp.,
1980. (Included by Reference).
- APPENDIX E -- "Reference Manual For Uniform Monitor Program MSC 8301",
Monolithic Systems Corp., 1978. (Included by Reference).
- APPENDIX F -- "Microcomputer Analog I/O Systems MP 8418", Burr-Brown
Research Corporation, 1978. (Included by Reference).

SOURCES

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